SUN HIGH TECH

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S U N E L E C T R I C E U R O P E

SERVICE MANUAL

FOR THE MCS-_20000SL

PRODUCED FROM NOVEMBER-91 ONWARDS

NOVEMBER-1991

PART NO : 0692E9307-87 **REV: A**

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SERVICE MANUAL

MCS-2000SL

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SECTION 1

INTRODUCTION

1.1 GENERAL INTRODUCTION

1.2 TECHNICAL SPECIFICATION

1.3 GENERAL MAINTENANCE

1.4 TESTER OPERATION (REMOTE-CONTROL)

THIS MCS/OCS-2000SL SERVICE MANUAL HAS BEEN DIVIDED INTO SECTIONS AS OUTLINED IN THE TABLE OF CONTENTS, EACH SECTION DEALS WITH A SPECIFIC ASPECT OF THE UNIT.

BEFORE SERVICING THE UNIT, THE OPERATING INSTRUCTIONS AS DESCRIBED IN THE OPERATOR'S MANUAL SHOULD BE FULLY UNDERSTOOD,

WHERE POSSIBLE THE ORIGINAL SERVICE MANUAL FOR A PARTICULAR ITEM HAS BEEN INCLUDED.

DURING SERVICING IT SHOULD BE FIRST ASCERTAINED AS TO WHETHER OR NOT THE UNITS POWER SUPPLIES ARE FUNCTIONING CORRECTLY.

AFTER CONFIRMING THE POWER SUPPLY, THE FAULT SHOULD BE TRACED USING THE SECTION COVERING THE SUSPECTED AREA IN WHICH THE FAULT IS OCCURRING,

GENERAL NOTES

1: DO NOT REMOVE BOARDS OR DISCONNECT ANY CONNECTORS WHILE THE POWER IS ON.

2: FOLLOW THE TROUBLE SHOOTING GUIDE'S DIRECTIONS CAREFULLY. DO NOT SKIP ANY STEPS OR MAKE ASSUMPTIONS.

3: PAY CLOSE ATTENTION TO THE DASH NUMBERS AND REVISION LETTERS OF THE BOARDS AND THE SOFTWARE,

4: SOME PROBLEMS MAY DISPLAY SEVERAL SYMPTOMS, IN THIS CASE LOOK FOR A SINGLE SYMPTOM WHICH LINK THE VARIOUS SYMPTOMS TOGETHER.

5: THE INSTRUCTIONS MAY REQUEST THAT YOU PERFORM A TASK WHOSE OUTCOME WILL DECIDE A SEQUENCE OF SUBSTITUTIONS. THIS SYSTEM FACILITATES THE MOST DIRECT ROUTE TO THE CAUSE OF THE PROBLEM, THE ORDER IN WHICH SUBSTITUTIONS ARE MADE IS BASED ON PROBABILITY AND THE EASE OF ACCESS.

6: BEFORE SUBSTITUTING ANY BOARDS CHECK THAT THE BOARDS AND CONNECTORS ARE FULLY SEATED.

7; THIS MANUAL IS PRIMARILY INTENDED FOR SERVICING THE MCS/OCS-2OOOSL FROM PRODUCTION NOVEMBER-91 ONWARDS (SYSTEM SOFTWARE V5.** OR HIGHER), TO SUB-UNIT LEVEL ONLY,

8: ALL DISKS SHOULD BE KEPT CLEAN AND DRY AND SHOULD BE STORED IN THE DISK STORAGE AREA OF THE TECH-15 CABINET.

CAUTION: MAGNETIC MATERIALS SHOULD BE KEPT AWAY FROM ALL DISKS TO **PREVENT POSSIBLE DAMAGE.**

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SAFETY PRECAUTIONS

GENERAL

THE TESTER IS SUPPLIED IN A SAFE CONDITION. IN ORDER TO KEEP IT IN A SAFE CONDITION AND TO ENSURE SAFE OPERATION OF THE TESTER, THE OPERATING INSTRUCTIONS MUST BE FOLLOWED AND THE WARNINGS & CAUTIONS MUST BE OBSERVED.

ABOUT WARNINGS

A WARNING GIVES INSTRUCTIONS TO PREVENT INJURY TO PEOPLE. WARNINGS WILL BE GIVEN IN THE FOLLOWING LIST AND JUST BEFORE THE SUBJECT IN THIS MANUAL WHERE THE WARNING IS APPLICABLE.

WARNINGS

1: BEFORE APPLYING MAINS POWER TO THE TESTER, MAKE SURE THAT THE POWER CABLE IS PLUGGED IN A PROPER POWER OUTLET. (REFER TO THE SERIAL NUMBER PLATE ON THE REAR OF THE CABINET FOR MAINS POWER REQUIREMENTS). A TOO HIGH VOLTAGE CAN DAMAGE THE TESTER AND RENDER IT UNSAFE.

2: ONLY USE FUSES WITH THE FUSE RATING WHICH IS INDICATED NEAR THE FUSE HOLDER. THE USE OF INCORRECT FUSES CAN DAMAGE THE TESTER OR THE POWER CABLE AND MAKE THESE ITEMS UNSAFE.

3: A. DO NOT MAKE CONNECTIONS TO A VEHICLE BEFORE THE MAINS CABLE OF THE TESTER IS CONNECTED TO THE PROPER SOCKET OUTLET.
B. PLUG THE MAINS CABLE IN A SOCKET OUTLET WITH A PROTECTIVE EARTH CONTACT.
C, DO NOT DISCONNECT THE MAINS CABLE BEFORE DISCONNECTING THE CONNECTIONS TO THE VEHICLE.
IF THE TESTER IS NOT CONNECTED TO EARTH DANGEROUS VOLTAGES CAN BE PRESENT ON THE CASING OF THE TESTER.

4: DO NOT OPEN THE CABINET. THERE ARE HIGH VOLTAGES AT SEVERAL POINTS INSIDE THE TESTER.

5: DO NOT OPERATE THE TESTER WHEN:
- IT IS WARMER THAN 40 °C
- IT IS COLDER THAN 5 °C
- THE RELATIVE HUMIDITY IS HIGHER THAN 80 %
WHEN THE TESTER IS USED BEYOND THESE OPERATING LIMITS ITS FUNCTIONALITY MAY DECREASE.
AT TEMPERATURES LOWER THAN -10 °C THE TESTER MAY BECOME UNSAFE.

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6: DO NOT OPERATE THE TESTER BEFORE CONTACTING THE LOCAL SUN SERVICE CENTRE, WHEN THE TESTER:

- SHOWS VISIBLE DAMAGE
- FAILS TO PERFORM THE INTENDED MEASUREMENTS
- HAS BEEN SUBJECTED TO PROLONGED STORAGE UNDER UNFAVOURABLE CONDITIONS
- HAS BEEN SUBJECTED TO SEVERE TRANSPORTATION STRESSES.

IT IS POSSIBLE THAT THESE CONDITIONS CAN MAKE THE TESTER UNSAFE.

7: ALWAYS PLACE WHEEL CHOCKS IN FRONT AND AT THE REAR OF THE DRIVE WHEELS BEFORE TESTING A VEHICLE. THIS IS TO PREVENT THE VEHlCLE FROM MOVING.

8: DO NOT INHALE EXHAUST GASES. WORK IN A PROPERLY VENTILATED AREA. EXHAUST GASES CONTAIN CARBON MONOXIDE (CO) WHICH IS A COLOURLESS AND ODOURLESS LETHAL GAS.

9: HIGH VOLTAGES ARE PRESENT ON THE SECONDARY SIDE OF THE IGNITION CIRCUIT WHILE THE ENGINE IS RUNNING. ALWAYS USE AN INSULATED PLIERS WHEN HANDLING THE IGNITION SYSTEM COMPONENTS.

10: WIPE UP FUEL SPILLS IMMEDIATELY AND DISPOSE OF SOAKED RAGS IN PROPER AIRTIGHT CONTAINERS. THE SOAKED RAGS PRODUCE FUMES WHICH ARE EXPLOSIVE.

11: NEVER SMOKE NEAR GASOLINE. GASOLINE FUMES ARE EXPLOSIVE.

12: DO NOT OPEN CLOSED COOLANT SYSTEMS WHILE THE FLUID IS HOT. STEAM WILL ESCAPE WHICH CAN CAUSE SERIOUS BURNS

13: NEVER LOOK DIRECTLY INTO THE CARBURETTOR THROAT WHEN CRANKING OF RUNNING THE ENGINE. BACKFIRING CAN CAUSE BURNS.

14: AVOID CONTACT WITH HOT SURFACES SUCH AS:

- EXHAUST MANIFOLDS AND PIPES
- MUFFLERS
- CATALYTIC CONVERTERS
- RADIATORS AND HOSES,

THESE CAN CAUSE SERIOUS BURNS.

15: NEVER USE A NAKED FLAME NEAR THE BATTERY. BATTERIES PRODUCE A HYDROGEN GAS WHICH EXPLODES WHEN IT COMES IN CONTACT WITH FIRE.

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16: ALWAYS KEEP A FIRE EXTINGUISHER IN THE WORK AREA. IT SHOULD BE SUITABLE FOR A RANGE OF USES INCLUDING GASOLINE. CHEMICAL AND ELECTRICAL FIRES.

17: DO NOT LAY TOOLS OR EQUIPMENT ON THE BATTERY. ACCIDENTAL SHORTING OF THE BATTERY TERMINALS CAN CAUSE SHOCKS AND BURNS, AND DAMAGE THE VEHICLE WIRING OR THE BATTERY ITSELF.

18: BATTERY ACID CAN DAMAGE CLOTHING AND BURN SKIN OR EYES. IF CONTACT IS MADE WITH BATTERY ACID, WASH THE AFFECTED AREA WITH AS MUCH WATER AS POSSIBLE AND USE A WEAK SODA (SUCH AS BAKING SODA) TO NEUTRALISE THE ACID. IF ACID ENTERS THE EYES, CONSULT WITH A DOCTOR OR A MEDICAL PERSON IMMEDIATELY.

19: SAFETY GOGGLES SHOULD BE ALWAYS WORN WHILE WORKING ON A VEHICLE TO PROTECT THE EYES FROM ACID, DUST. GASOLINE AND ANY OTHER LOOSE OBJECTS THAT MAY COME FROM ANY MOVING PARTS.

20: DO NOT WEAR A NECKTIE, SCARF OR LOOSE CLOTHING NEAR AN OPERATING ENGINE. KEEP HANDS AND HAIR AWAY FROM MOVING ENGINE PARTS SUCH AS FAN BLADES, BELTS OR PULLEYS. THESE CAN CAUSE A SERIOUS INJURY.

21: NEVER WEAR WRIST WATCHES, RINGS OR OTHER JEWELLERY WHEN WORKING ON A VEHICLE. SUCH ITEMS MAY CATCH ON MOVING PARTS OR CAUSE AN ELECTRICAL SHORT CIRCUIT WHICH CAN BURN OR INJURE THE WEARER.

22: DO NOT OPERATE THE TIMING LIGHT TOO NEAR FANS OR BELTS. THE TIMING LIGHT HAS THE EFFECT OF MAKING THE FAN SEEM TO "STAND STILL". THIS IS A DANGEROUS OPTICAL ILLUSION WHICH MIGHT CAUSE THE OPERATOR TO CONTACT THE FAN.

23: KEEP HANDS AND OTHER OBJECTS AWAY FROM THE ELECTRIC COOLING FAN. THE FAN CAN START UP AT ANY TIME.

****

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ABOUT CAUTIONS

CAUTIONS GIVE INSTRUCTIONS TO PREVENT DAMAGE TO EQUIPMENT. CAUTIONS WILL BE GIVEN IN THE FOLLOWING LIST AND JUST BEFORE THE SUBJECT THE CAUTION' IS APPLICABLE.

CAUTIONS

1: CHECK THE ENGINE OIL LEVEL AND ADD OIL IF NECESSARY BEFORE PERFORMING ANY TEST. AN ENGINE SHOULD NOT BE TESTED IF THE OIL LEVEL IS TOO LOW.

THE TEST RESULTS WILL BE INFLUENCED AND THE ENGINE CAN BE DAMAGED IF A TEST IS PERFORMED WITH A LOW OIL LEVEL.

2: CHECK' THE COOLANT LEVEL AND ADD COOLANT IF NECESSARY BEFORE: PERFORMING ANY TESTS. AN ENGINE SHOULD NOT BE TESTED IF THE COOLANT LEVEL IS TOO LOW.

IF THE ENGINE IS HOT, CHECK THE LEVEL AT THE OVERFLOW TANK. THE TEST RESULTS WILL BE INFLUENCED AND THE ENGINE CAN BE DAMAGED IF A TEST IS PERFORMED WITH A LOW COOLANT LEVEL.

3: FOLLOW THE CAR MANUFACTURER'S INSTRUCTIONS WHEN WORKING ON VEHICLES WITH A CATALYTIC CONVERTER.

THE CONVERTER CAN BE DAMAGED BY BACKFIRES OR BY TOO MUCH UNBURNED FUEL GETTING INTO THE EXHAUST SYSTEM.

4: KEEP THE TEST LEADS AWAY FROM HOT SURFACES OR MOVING ENGINE PARTS. THE TEST LEADS CAN NOT WITHSTAND HIGH TEMPERATURES OR SEVERE MECHANICAL STRESS.

****

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TECHNICAL SPECIFICATIONS:

SUITABLE FOR TESTING 2, 3, 4, 5, 6 AND 8 CYLINDER ENGINES.

TACHOMETER	0 . . ...9999 RPM AUTORANGING BARGRAPH
TIMING LIGHT	0 . ...90 DEG
TDC SENSOR	-20 . . . ..+180 DEG
DWELL	0 . ...180 DEG
FIRING VOLTAGE	0 . ...50 KV
SPARK VOLTAGE	-lO....+lOkV
SPARK DURATION	0 . . ..lOmS
DISTRIBUTOR-VOLTAGE DROP	-2o....+20V
COIL INPUT VOLTAGE	-2o....+20V
BATTERY VOLTAGE	-40,...+40V
ALTERNATOR RIPPLE	0 . . ..10%
CURRENT	-100.... +lOO AMP -500....+500 AMP
VACUUM	0 . . ..1000mB
OIL TEMPERATURE	-10.. 150 DEG
PIN POINT VOLTAGE	-40....+40V FAST RESPONSE BARGRAPH
PIN POINT OHMS	0. . ..250kOhm AUTO RANGING FAST RESPONSE BARGRAPH

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THE MCS-2000 IS A PRECISION MEASURING SYSTEM THAT REQUIRES LITTLE MAINTENANCE. HOWEVER TO ENSURE TROUBLE FREE OPERATION THE FOLLOWING AREA'S OF THE SYSTEM SHOULD BE CHECKED AS A MATTER OF ROUTINE DURING EVERY VISIT OF THE SERVICE ENGINEER.

THIS MAINTENANCE **MUST** BE CARRIED OUT PRIOR TO CALIBRATION OR REPAIR.

A. COMPLETE TESTER

B. FLOPPY DISC DRIVE(S)

C. LEADS AND PICK-UPS

D. INFRA RED GAS BENCH (OPTION)

E. PRINTER (OPTION)

F. DIESEL (OPTION)

G. STL-2 (OPTION)

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A. COMPLETE TESTER

STEP 1 FAN FILTER MAINTENANCE

REMOVE AND CLEAN THE FAN FILTER (LOCATED ON THE REAR OF THE TESTER) USING COMPRESSED AIR.

STEP 2 CLEAN TESTER

IF NECESSARY CLEAN TESTER WITH A DAMP CLOTH.

B. FLOPPY DISC DRIVE(S)

FLOPPY DISC DRIVE(S) ARE MAINTENANCE FREE.

C. LEADS AND PICK-UPS

STEP 1 INSPECT AND IF NECESSARY REPLACE/REPAIR ANY DAMAGED LEADS OR PICK-UP'S.

D. INFRA-RED GAS BENCH (OPTION)

STEP 1 SAMPLE HOSE MAINTENANCE

INSPECT THE SAMPLE HOSE FOR ANY SIGN OF DAMAGE SUCH AS LEAKS, CUTS, KINKS ETC- BLOW OUT THE SAMPLE HOSE WITH COMPRESSED AIR TO REMOVE ANY DIRT OR CONDENSED WATER. IF NECESSARY REPLACE SAMPLE HOSE.

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STEP 2 SAMPLE PROBE MAINTENANCE

INSPECT THE SAMPLE PROBE FOR DAMAGE OR BLOCKAGE.IF NECESSARY USE A PIECE C STIFF WIRE TO DISLODGE AND REMOVE ANY FOREIGN MATTER.

STEP 3 SAMPLE FILTER MAINTENANCE

INSPECT THE PRIMARY AND SECONDARY FILTERS CLEAN AND/OR REPLACE AS NECESSARY. ENSURE FILTER BOWLS ARE SEATED CORRECTLY. SEE **PAGE 13** FOR SAMPLE FILTER ASSY DETAILS.

E. PRINTER (OPTION)

THE PRINTER IS MAINTENANCE FREE, FOR RIBBON AND PAPER CHANGING SEE 5.2.

F. DIESEL (OPTION)

INSPECT THE INNER SURFACE OF THE PIEZ0 ELECTRIC PICK-UP FOR SCORING. SHOULD THIS SURFACE BE DAMAGED IT MAY BE NECESSARY TO REPLACE THE PICK-UP.

IMPORTANT

UNDER NO CIRCUMSTANCES SHOULD THE PICK-UP BE ROTATED ONCE IT IS CLAMPED TO A FUEL LINE.

G. STL-2 (OPTION)

SEE STL-2 SERVICE/REPAIR MANUAL.

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SAMPLE FILTER ASSEMBLIES

FILTER MAINTENANCE

WHEN THE "LOW FLOW/CHECK fILTER" WARNING LIGHT COMES ON **DURING VEHICLE TESTING. THE SAMPLE FILTERS MUST** DE SERVICED.

WHEN SERVICING FILTERS. BE SURE THAT ALL SEALS ARE PROPERLY POSITIONED AND THE UNITS ARE RE-ASSEMBLED SNUGLY TO ELIMINATE THE POSSIBILITY Of **OUTSIDE AIR BEING DRAWN INTO THE ANALYZER DURING** VEHICLE TESTS.

PRIMARY FILTER SERVICE

(ELEMENT SHOULD BE CLEANED OR **REPLACED** AS **NECESSARY)**

Note: OBSERVE **FILTER** FROM **BOTTOM**

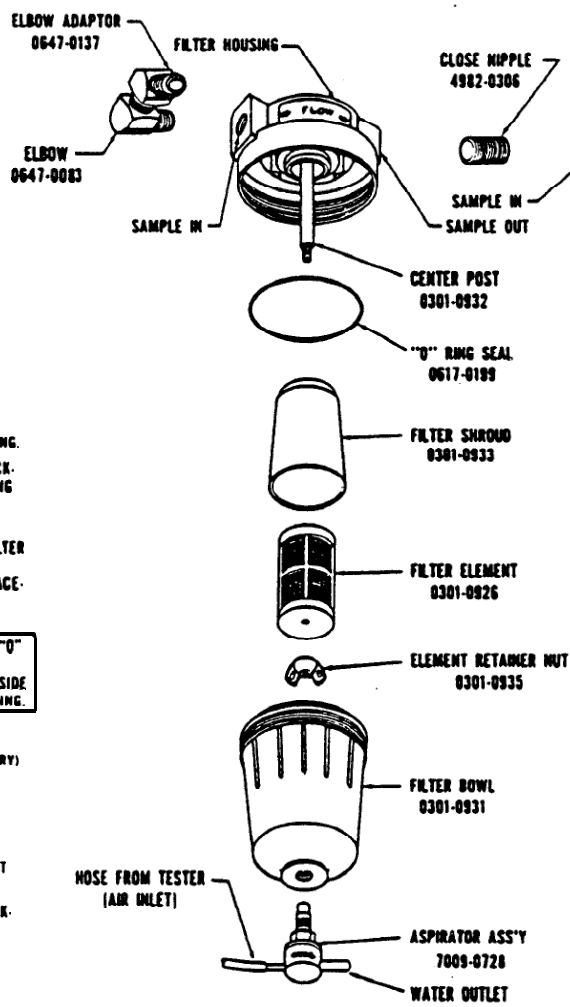
1. **REMOVE OUTLET AND INLET** NOSES **FROM "T" FITTING** OR LOWER **PART** Of **FILTER BOWL.**
2. REYOVE **FILTER BOWL FROM HOUSING BY TURNING IT COUNTER CLOCKWISE.** ROTE **POSITION** Of **"O" RING SEAL** OR **FILTER HOUSING.**
3. TURN **ELEMENT RETAINER NUT** COUNTER **CLOCK-WISE AND REMOVE FILTER ELEMENT BY PULLING DOWNWARD** OR **FILTER SHROUD IN A TURNING MOTION.**
4. **CLEAN FILTER BOWL. FILTER ELEMENT. AND FILTER SHROUD IN A SOLUTION** Of **DETERGENT AND WATER AND THEN** AIR **DRY. IF ELEMENT REPLACE-MENT IS NECESSARY. USE SUN NO. 0301-0926** FILTER ELEMENT.
5. **ASSEMBLE IN** REVERSE **ORDER MAKING** SURE **"O" RING** IS **PROPERLY POSITIONED IN GROOVE IN FILTER HOUSING. RECONNECT INLET HOSE TO SIDE OF "T" FITTING THAT HAS THE SMALLEST OPENING.**

SECONOARY FILTER SERVICE

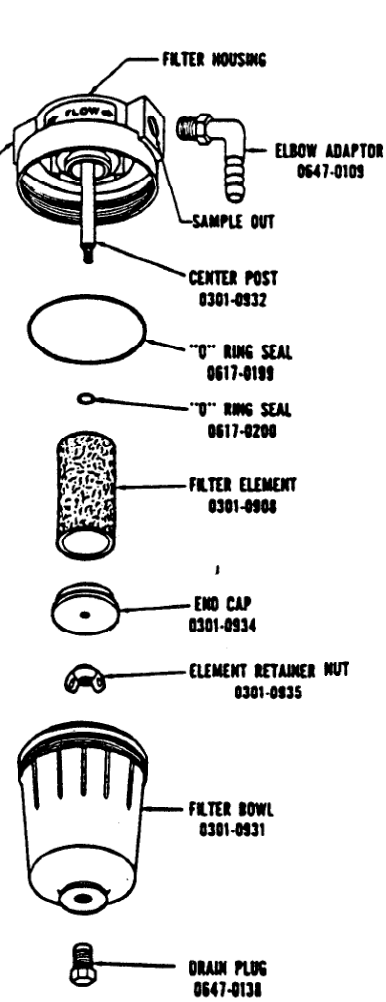
(ELEMENT SHOULD BE REPLACED AS NECESSARY)

Note: OBSERVE FILTER FROM **BOTTOM**

1. **REMOVE FILTER BOWL FROM HOUSING BY TURNING IT COUNTER CLOCKWISE.**
2. **INSPECT "O" RINGS ON FILTER HOUSING SHAFT AND FILTER HOUSING.**
3. **TURN ELEMENT RETAINER NUT COUNTER CLOCK-**WISE **AND REMOVE FILTER** ELEMENT
4. REYOVE **FILTER ELEMENT AND REPLACE WITH SUN NO. 0301-0908 ELEMENT. (DO** ROT ATTEMPT **TO CLEAN)**
5. WASH **FILTER BOWL IN A SOLUTION** Of **DETERGENT AND WATER AND THEN AIR DRY.**
6. **ASSEMBLE IN REVERSE ORDER MAKING SURE ALL "O" RINGS** ARE **PROPERLY POSITIONED.**



PRIMARY FILTER ASSEMBLY
75 MICRONS
0301-0115



SECONDARY FILTER ASSEMBLY
8 MICRONS
0301-0116

0682-0539-02 REV. 9

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NEW REMOTE CONTROL 1.4

The new remote control for the MCS/OCS testers is similar to the MEA-1500 remote control.

The new keypad (MEA) uses three lines more than the old pad. Besides that all other lines have different pin-locations.

An addition of two lines was necessary because there was one unused line in the old situation

This unused line is re-pinned (see schematic of dig.i/o-pcb and system wiring 1/3).

The new keypad is the same as the MEA keypad, but the keypad-connector has other pin locations.

So the new MCS or OCS remote control are not compatible with the MEA remote control.

WARNING:

SERVICE-DISK V 4.20 CAN ONLY BE USED WITH THE OLD REMOTE CONTROL ! (TESTER CONFIGURATION MAY BE FOR MEA KEYPAD).

SERVICE-DISK V 5.** CAN HANDLE BOTH REMOTE CONTROLS (AS CONFIGURATED),

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USE:

The new keypad can be used in:

- **all test functions (like MCS-pad)**
- **special functions program selections (to Multimeter/ Scope/SDL)**
- **special functions in Scope**

All old keys have their equivalent on the new keypad,

Besides that some extra keys are used:

#	**to SDL**
CE	**to MCS/OCS**
?	**help**
V	**ignition scope: primary**
RIPPLE	**to digiscope / digiscope mode**
RASTER	**ignition scope: 1 cyl. / swapping**
V/KV	**ignition scope: chance V to KV**
.	**multimeter and scope: to last workshop test**
V/OHM	**to multimeter test (when vehicle is defined)**
KV	**ignition scope: secondary**
PARADE	**ignition scope: parade**
PERCENT	**ignition scope: 1 cyl, continuously**
mS	**scope: change X-ax**

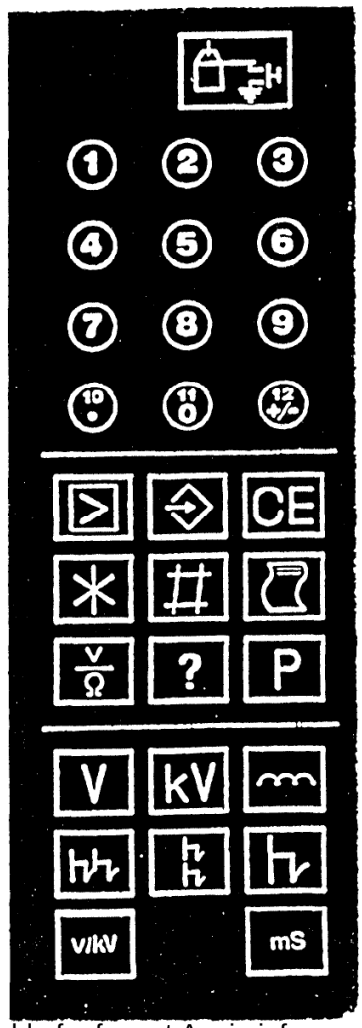
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NEW REMOTE CONTROL WIRING TABLE

BOOM J-408	W4 + W4-REM WIRE COLOUR	DIGITAL I/O J-205	COMMENTS:
	SCREEN	-	W4-REM TO SOLID CHASSIS GND
1	SCREEN	-	TO SOLID CHASSIS GROUND
2	WHITE/BLACK	D	MOVED FROM J-205, PIN 15
3	RED	1	W4-REM ADDED, J-205, PIN 4
4	BLACK	10	
5	BROWN	9	
6	RED	L	
7	ORANGE	K	
8	N.C.	-	
9	BLACK	13	W4-REM ADDED, J-205, PIN 13
10	YELLOW	N	
11	GREEN	11	
12	BLUE	M	
13	VIOLET	R	
14	WHITE	14	

CONNECTOR J-205 PIN LOCATIONS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	B	C	D	E	F	H	J	K	L	M	N	P	R	S



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SECTION 2

SERVICE INFORMATIONN

2.1 SERVICE DISK V4.20

2.2 SERVICE DISK V5.00

2.3 ERROR AND INTERRUPT CODES

2.4 SET-UP

2.5 CALIBRATION

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INTRODUCTION

Modifications to the service disk made for release V4.20:

The V4.20 Service Disk is a separate disk that is compatible with System V4.2. The purpose of this disk is to provide facilities for factory end-of-line and field service testing.

This disk as of MCS System V5.0 is the only way the tester hardware configuration can be defined. The disk can be used for testers using System software up to V4.2. Some configuration definitions for System 5.0 are also defined with this version.

The following is a description of all functional changes of the service software for this release:

- The service program now resides on a floppy disk instead of EPROM.

- The program has been completed upgraded to be compatible with MCS-System 4.2.

- New EEPROM entries added:
  - Definitions added for:
    - BAROMETER
    - KEYBOARD
    - RTC
    - SDL-20
  - KEYPAD option added:
    - MEA

- Removed the 'Gas bench' and 'Printer' definition in the configuration entry, They are now defined through the option entry.

- In the option entry, the EEPROM is updated only when an entry is modified.

- The tester warm up has been removed on power up. The tester comes straight into program select.

- Added 'Tester Calibration' entry in the main menu. This includes a warm up, self-test and calibration.

- Gas modules used are now identical to those that can be found on the V4.20 System Disk.

- 'Gas bench special functions' now has a menu entry to perform gas calibration.

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This manual gives an overview of the Service Disk and the test procedures that are available. The flow is listed in the diagrams. These diagrams may contain a sub-menu selection, a page to enter data or a test page.
Each of these sub-menus may lead to another sub-menu, an entry page or a test page.

Indexing method

All titles are indexed through a simple indexing methode- All sub-menu's and tests are prefixed with a string containing the following identifiers:

- a shortcut of the name of the calling menu
  (ex. FAT for FActory Test)
- and a number which designates the index into that menu.
  (ex. .2. is the secondary entry)

Put together: FAT.2 == secondary menu entry in the factory menu == Analog Rack Test

Diagrams

The diagrams that represent the pages of the tester are not necessarily exactly the same as those that can be found on the tester,

Values in the layouts do not represent any real tester value. Therefore these values should NOT be interpreted in any way; they merely serve as to give an indication of how the tester display looks during a test.

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MAIN MENU

The following menu entries are available on the Service Disk Version 4.20 in the main menu.

Menu layout:

```
MAIN;
[1]  |   TESTER CONFIGURATION ENTRY
[2]  |   GAS CALIBRATION
[3]  |   GAS BENCH SPECIAL FUNCTIONS
[4]  |   CUSTOMER MESSAGE EDITOR
[5]  |   LANGUAGE SELECTION
[6]  |   VEHICLE QUICK TEST
[7]  |   FACTORY TEST
```

MM-1 Tester Configuration Entry

This page contains a number of selections, Each selection can be DEFINED or NOT DEFINED. The selections are saved in EEPROM when this pages is left.

Menu layout:

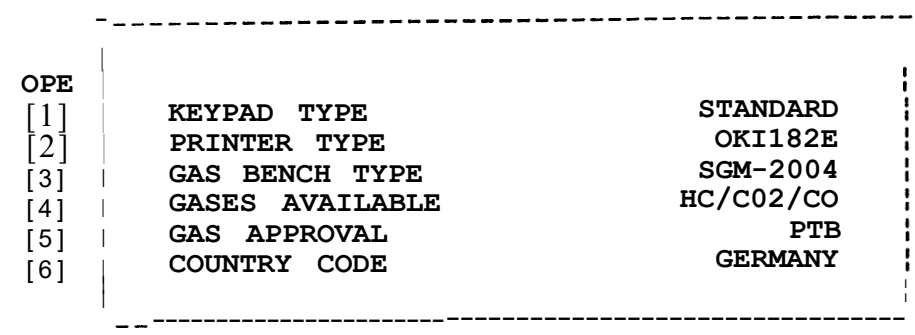
```
TCE  |
[1]  |   DIESEL OPTION              NOT DEFINED  |
[2]  |   DIAGNOSTICS                NOT DEFINED  |
[3]  |   TECH-15                    NOT DEFINED  |
[4]  |   DIGITAL SCOPE                  DEFINED  |
[5]  |   BAROMETER                      DEFINED  |
[6]  |   KEYBOARD                   NOT DEFINED  |
[7]  |   REAL-TIME CLOCK                         |  <- NOT USED YET
[8]  |   SDL-20                                  |  <- NOT USED YET
```

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MM.1 Option Entry

The Option Entry page allows for configuring the tester with specific hardware devices, Through selections, various types of equipment can be selected.

Menu layout:



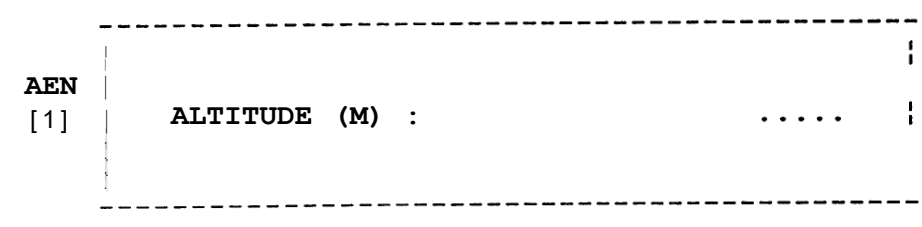
MM.2 Gas Calibration

Depending on the definition of the BAROMETER configuration, one of two different pages is entered.
The pages are:
- Altitude entry
- Barometric pressure display

GAC.1 Altitude Entry

The first page, entered when BAROMETER is NOT DEFINED, gives the user the possibility to set the current altitude before entering the gas calibration page.

Page layout:



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GAC.2 Barometric Pressure Display

Alternatively, when the BAROMETER is DEFINED, calibration of the barometer can be performed. The page enables the user to correct the input voltage of the barometer. The immediate calculated barometric pressure is also displayed.

Page layout:

```
BPD
[1]   BAROMETER    (VOLT)    .....
[2]   PRESSURE     (MBAR)    .....
```

After going through one of the previous pages, the gas calibration page is entered. In this page the user can calibrate the gas module hardware.

GAC.3 Gas Calibration

By following the instructions, given when this page is entered, the hardware can be calibrated.

Page layout:

```
                  ZERO        GAS         SPAN
                VOLTAGE     VALUES      VOLTAGE
GAC
[1]    CO         ....        .... %      .....
[2]    HC         .....       .... PPM    .....
L-31   CO2        .....       .... %      .....
[4]    02         ....        .... %      .....
```

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GAC.4 Tester Calibration

When the final adjustments are made in the previous page, the tester is re-calibrated. The tester calibration page is entered and all relevant calibrations are done.

MM.3 Gas bench special functions

The gas bench special functions entry is the same as the entry that can be found on the regular System Disk.
The number of sub-menus that can be found in this entry depents the type of the installed gas bench and/or whether barometric pressure compensation is installed.

#1 Menu layout APK approval test:

```
     ------------------------------------------------
 [1] |   MODULE DISPLAY                             |
 [2] |   APK APPROVAL                               |
     ------------------------------------------------
```

#2 Menu layout PTB and NO barometric pressure:

```
     ------------------------------------------------------------
 [1] |   MODULE DISPLAY                             |
 [2] |   PTB APPROVAL                               |
 [3] |   ALTITUDE ENTRY                             |
     ------------------------------------------------
```

#2 Menu layout PTB with barometric pressure:

```
     ------------------------------------------------------
 [1] |   MODULE DISPLAY                             |
 [2] |   PTB APPROVAL                               |
     ------------------------------------------------------
```

Other cases :

```
     ------------------------------------------------------------------
 [1] |   MODULE DISPLAY                             |
 [2] |   ALTITUDE ENTRY                             |
     ------------------------------------------------
```

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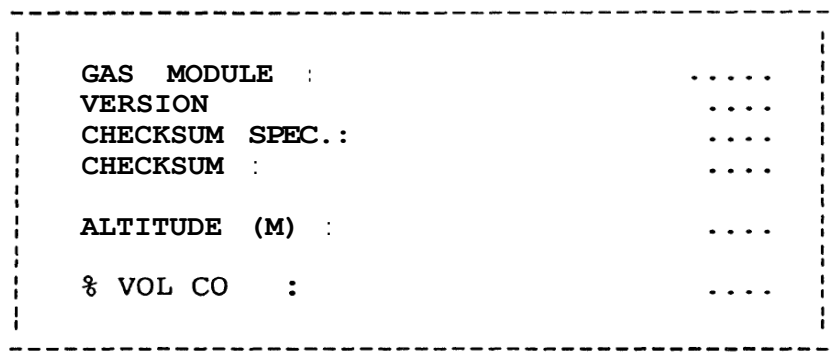
GSF.1 Module display

The module display shows a number of charcteristics of the gasmodule installed. The name and version number come directly from the gas bench software.
The checksum displayed is the one that is hardcode into the software. This checksum is always the same for a certain relese version of a gas bench.



GSF.2 PTB gas analyser check

Page layout:

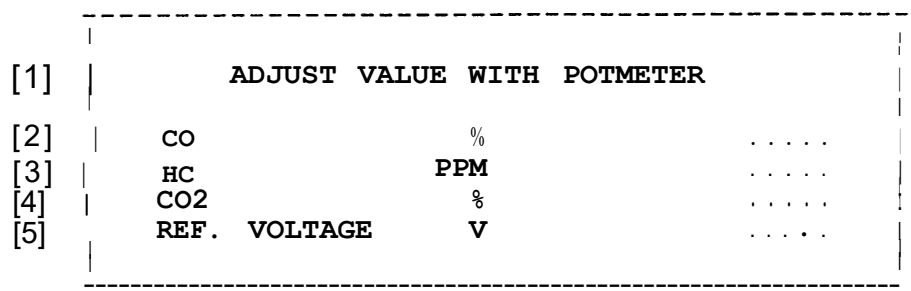


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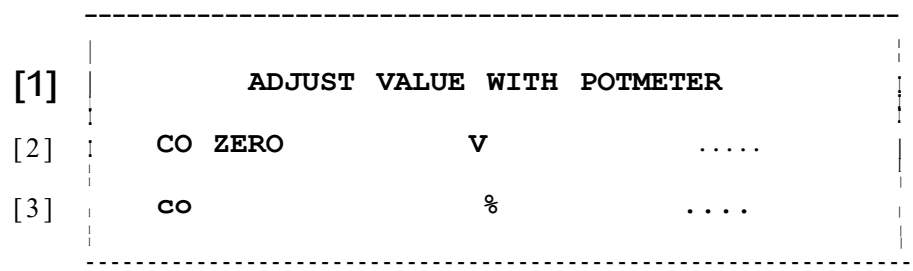
GSF.2 APK gas analyser check

When an ANDROS (SGM 2004) gas bench is installed, the APK gas analyser check is somewhat different then when another gas bench is installed.

Page layout:



Page layout for APK with ANDROS:



MM.4 Customer Message Editor

In this page, a message can be entered onto the screen. This message will be saved in EEPROM and can be obtained at a later time, even when the tester has been turned off.

MM.5 Language Selection

Page to select another language from disk, When another language is available, this pages allows the user to select another language (or the one that is currently in use), and load it into memory, After this, all text on the tester will be displayed in the newly loaded language.

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MM.6 Vehicle Quick Test

This pages leads the user the the vehicle entry screen. This page allows a general selection of a type of engine under test.

Menu layout:

```
VEE
[1]   ENGINE TYPE:                    LPG
[2]   NUMBER OF CYLINDERS:              4
[3]   FIRING ORDER:           1- 3- 4- 2

[4]   CYLINDER STROKE:                  4
[5]   MAG PROBE:                      YES
[6]   TDC OFFSET:                   -20.0
```

The next page that is entered is dependent of the fact whether a digital SCOPE is DEFINED or NOT DEFINED. If DEFINED, the next page shows the following options:

Menu layout:

```
VQT
[1]   MULTIMETER TEST
[2]   SCOPE FUNCTIONS
```

Otherwise, the first [1] options, MULTIMETER TEST, is directly entered.

VQT.1 Multimeter tests

The multimeter test pages are the same as the pages that can be found on the MCS System Disk.

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Multimeter test 1

Page layout:

ML1			
[1]	ENGINE	RPM	.....
[2]	BATTERY	VOLTS	.....
[3]	ALT RIPPLE	%	.....
[4]	CURRENT	AMPS	....
[5]	COIL +/KL.15	VOLTS	....
[6]	COIL -/KL.1	VOLTS	.....
[7]	DWELL		.....
[8]	PEAK FIRING VOLTAGE	KV	.....
[9]	HC	PPM	.....
[10]	OIL TEMPERATURE	C	.....

Multimeter test 2

Page layout:

[1]	ENGINE	RPM	.....
[2]	TIMING		.....
[3]	DWELL		.....
[4]	PEAK FIRING VOLTAGE	KV	.....
[5]	VACUUM	MBAR	.....
[6]	OIL TEMPERATURE	C	.....

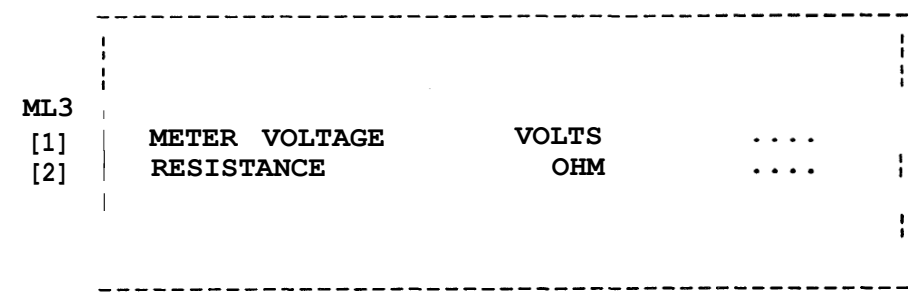
Secondary page layout:

[1]	ENGINE	RPM	.....
[21]	CO	%	.....
[3]	HC	PPM	.....
[4]	CO2	%	.....
[5]	O2	%	.....
[6]	LAMBDA CALCULATED		.....
[7]	AIR FUEL RATIO		.....
[8]	OIL TEMPERATURE	C	.....

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Multimeter test 3

Page layout:



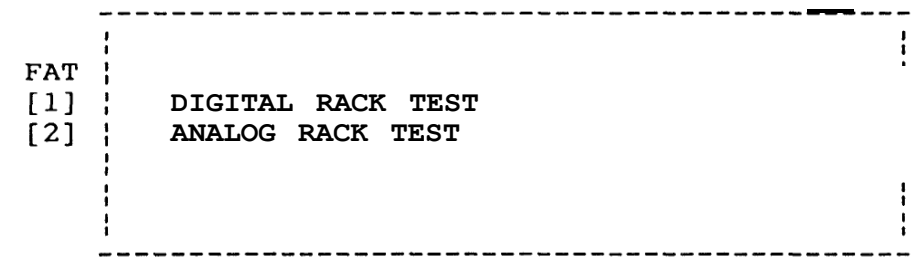
VQT.2 Scope functions

The scope functions are identical to those that can be found on the System Disk.

MM.7 Factory test

The factory test menu entry takes us to the basic selection of the service tests. The testing of the computer system is divided into two main categories.
The first part is the digital rack test. This is for testing all digital functions of the tester.
Secondly, there's the option to test the analog circuitry of the tester,

Menu layout:

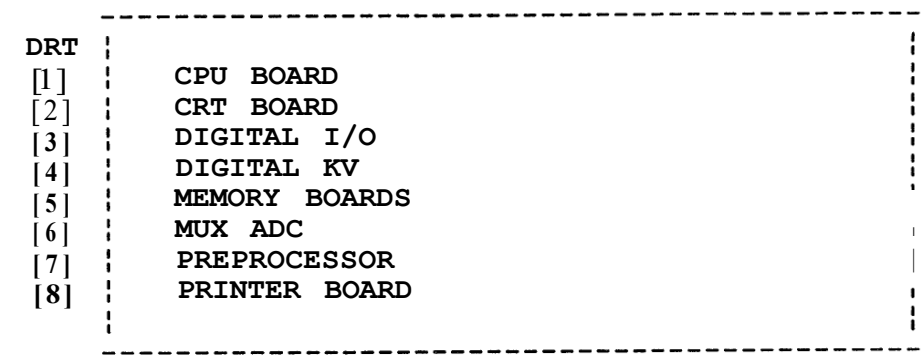


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FAT.1 Digital Rack Test

Sub-menu's and test page entries for testing of boards in the digital boards rack.

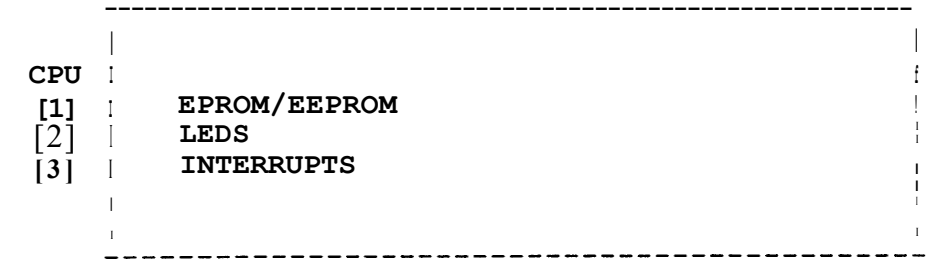
Menu layout:



DRT.1 CPU board

The CPU board test contains three entries. Each of them serves to monitor the functioning of a specific part of the CPU board of the tester.

Menu layout:



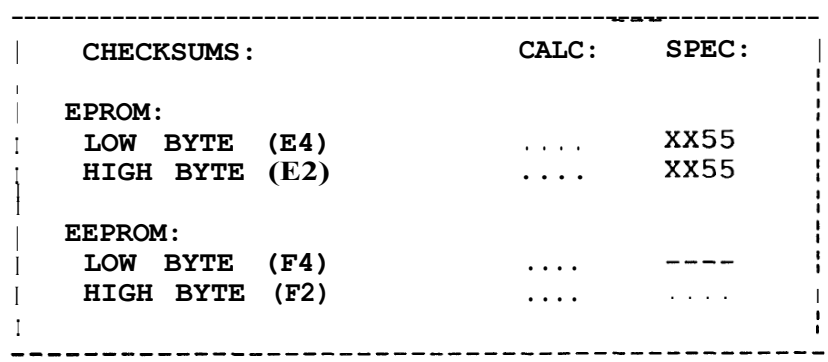
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CPU.1 EPROM/EEPROM

The page shows the checksum of the EPROM and EEPROM. The checksums indicate if the information contained in the respective PROM's is reliable.

For the EPROM the least significant byte should always be 0x55h.

Page layout:



Legend:

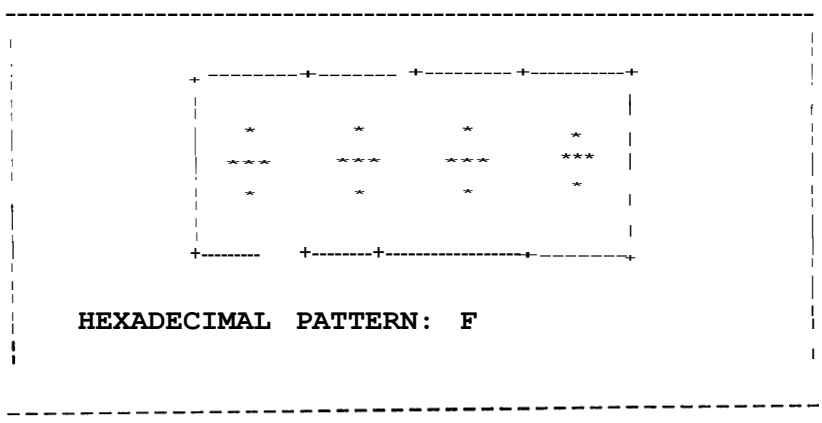
xx	means	: No specificastion
-_--	means	: Specification not possible because low byte is not used in this configuration

CPU. 2 Leds

The leds test enables the user to individually activate any of the four leds that are mounted on the CPU board. By stepping through the varous input values, a different pattern is displayed. This pattern is from left to right the hexadecimal value that is entered,
(Led on means '1')

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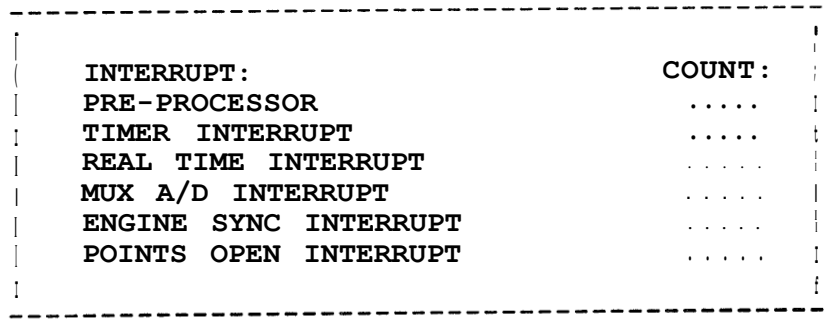
Page layout:



CPU.3 Interrupts

The interrupts test continuously displays a number of counters. Each counter shows the total number of interrupts that the CPU received since the test page was entered. While in the test page, the counters are continuously updated. Each of the counters displays the number of interrupts that a specific hardware devices generates.

Page layout:

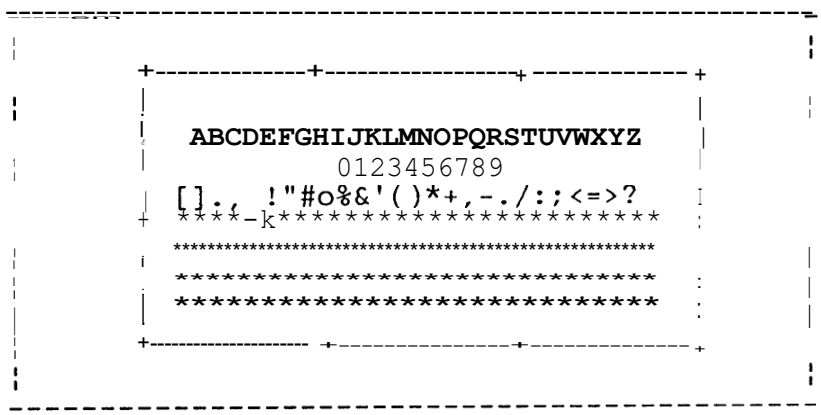


DRT.2 CRT CONTROLLER BOARD

The cathode ray tube test is designed to test the CRT RAM. The RAM is tested by writing a value to RAm and subsequently read that RAM location. Whenever different values are found, a CRT Failure message will be displayed.

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Test page layout:



DRT.3 Digital I/O

The digital I/O test contains tests that communicate through digital I/O ports. These ports/lines can be tested directly-

Menu layout:



DIO.1 Keypad

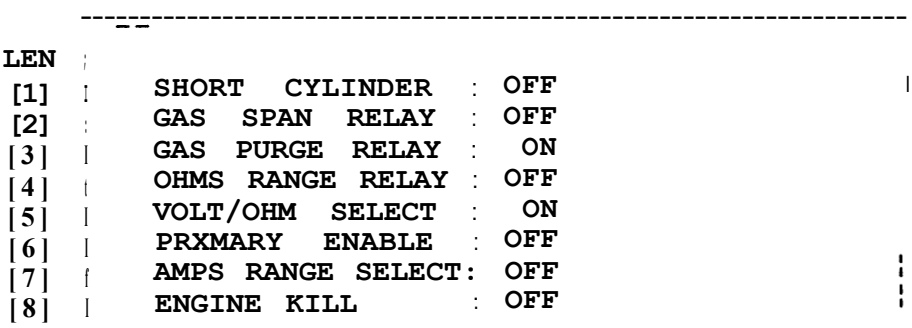
The display contains the layout of the standard MCS keypad. By pressing a key on the keypad (except for 'P'), the actual functioning of the key can be checked.

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DIO.2 Line Enable

Test digital I/O lines. The line can be tested by setting a '1' or a '0' on the output.

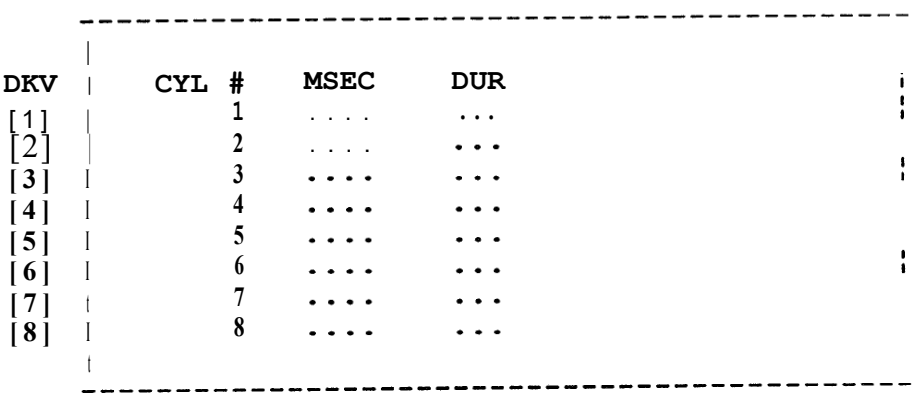
Test page layout:



DRT.4. Digital KV board

Measurement of interval (dwell) after cylinder firing for each cylinder. The number of cylinders is fixed at 8.

Page layout:

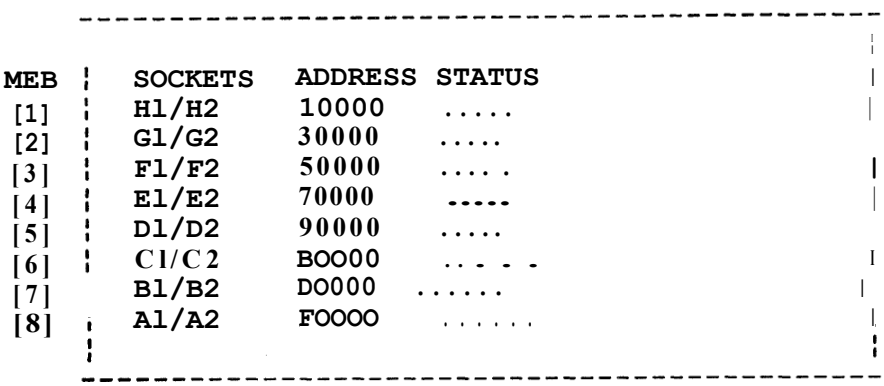


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DRT.5 Memory board

The system RAM can be tested in this page.

Page layout:



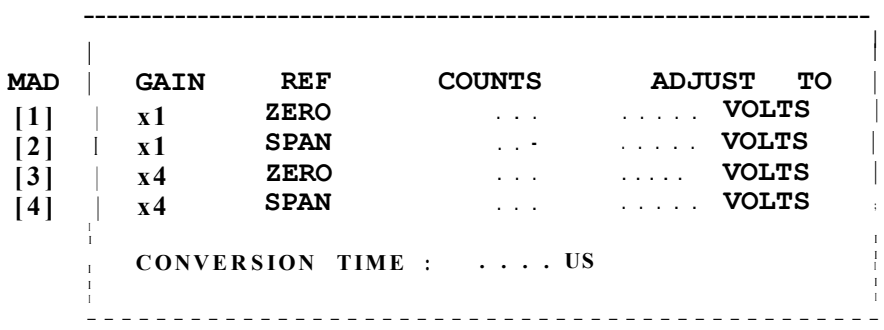
Status can be one of the following:

- TESTING : busy testing the RAM socket
- GOOD : RAM socket test succeeded
- INCOMPLETE : testing RAM socket skipped by pressing '#'
- ****:****:**** : failure detected at this address

DRT.6 MUX ADC board

Test zero (0) and span (2000) of ranges 1.835 and 7.350 Volts each.

Page layout:



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DRT.7 Preprocessor board

Three selections can be made in the preprocessor board test.

Menu layout:

```
PPB
[1]   PREPROCESSOR STATUS
[2]   PREPROCESSOR READINGS
[3]   SHORT CYLINDER TEST
```

PPB.1 Preprocessor status

In this page the status of the preprocessor is displayed.

Page layout:

```
PPS
[1]   ENGINE SYNCHRONIZATION  :  ON
[2]   MAGNITUDE SIGNAL        :  OFF
[3]   CYLINDER CLOCK          :  ON

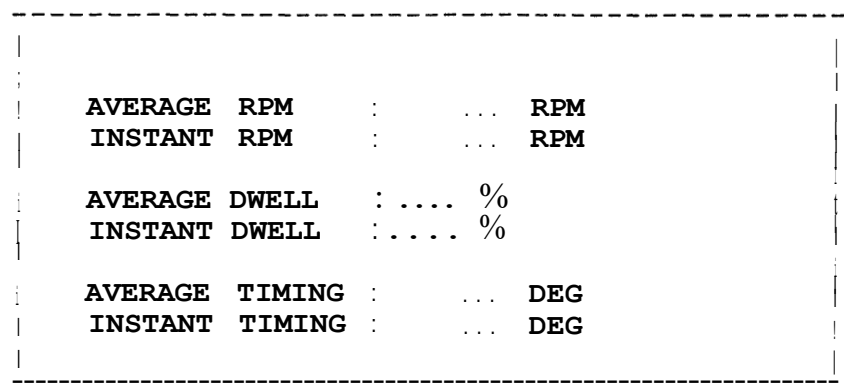
[4]   NUMBER OF CYLINDERS DETECTED: 4
```

PPB.2 Preprocessor readings

Display current readings of the preprocessor.

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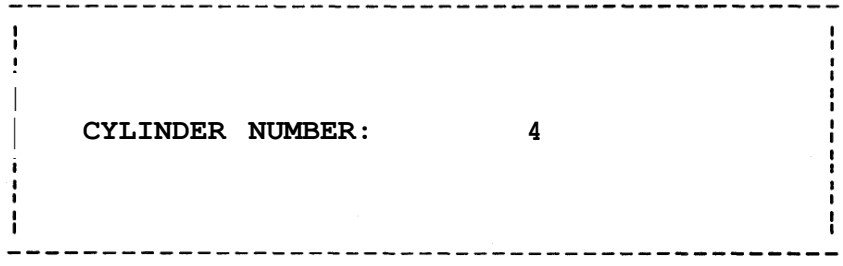
Page layout:



PPB.3 Short cylinder test

Enter cylinder numbers in terms of firing order. The cylinder selected will instantly be shorted.

Page layout:



DRT.8 Printer board

Test Printer Board. Pressing the printkey when in this page will send all characters from the display memory to the printer.

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FAT.2 Analog Rack Test

Secondary sub-menu of factory testing_ This page shows the possible entries of pages that lead to various tests of analoge parts of the tester.

Menu layout :

```
      ------------------------------------------------
      |                                              |
 ART  |                                              |
 [1]  |    AMPS BOARD                                |
 [2]  |    VOLT/OHM                                  |
 [3]  |    PEAK KV/RIPPLE                            |
 [4]  |    SPARK KV/SLOPE                            |
 [5]  |    BOOM POD                                  |
 [6]  |    TRIGGER PRIMARY                           |
      |                                              |
      ------------------------------------------------
```

ART.1 Amps board

Select Amps 100 or Amps 1K range and test MUX voltage. The values read are displayed in two formats: a raw value, directly read and display and an average value.

Page layout:

```
      ------------------------------------------------
      |                                              |
      |                      VALUE          MUX      |
 AMP  |                                    VOLTAGE   |
 [1]  |    AMPS 100 ZERO                    ......    |
 [2]  |    RAW AMPS                         ......    |
      |                                              |
 [3]  |    AVERAGE AMPS        ...          ......    |
      |                                              |
      ------------------------------------------------
```

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ART.2 Volt/Ohm board

Select MVOLT or OHMS and test MUX voltage :

Page layout:

VOB		VALUE	MUX ZERO	VOLTAGE READ
[1]	VOLTS V	...	.....	...*
[2]	OHMS			.....
[3]	OHMS OPEN			.....
[4]	ZEROHMS			.....

ART.3 Peak kv/ripple

Test MUX voltages for the peak KV test.

Page layout:

PKV		VALUE	MUX ZERO	VOLTAGE READ
[1]	PKKV KV		.....	.....
[2]	RIPPLE V	..:::	.....	.....
[3]	%	...	.....	.....
[4]	BATTERY V	...		.....

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ART.4 Spark kv/slope

Page layout:

	VALUE	MUX ZERO	VOLTAGE READ
SKS			
[1]	Spark 1 KV	.....	.....
[2]	Spark 2 KV	.....	.....

ART.5 Boom pod

Test the boom pod. The values are read from the inputs and displayed directly on the screen.

Page layout:

	VALUE	MUX ZERO	VOLTAGE READ
BP0			
[1]	KL.1 V ...		.....
[2]	KL.15 V		.....
[3]	BATT. V :::		.....
[4]	VACUUM mB .	.....	.....
[5]	OIL T. C ..		.....

ART.6 Calibration

This page is identical to the Main menu option 2: MM.2 entry GAC.4 .

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S U N E L E C T R I C E U R O P E

THE MCS-2000 SERVICE DISK MANUAL

SOFTWARE VERSION: V5*03

(P/N: 0553E1075-01)

JANUARY-1992

NOTE
Service disk 5.03 was replaced by service disk 5.10
Part No. 0553e1075 11
The instruction sheet was not reissued

PART NO: 0692E9308-17 REV: A

REF FILE: MCS-SM.DOC REF: ERN 0729

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MCS-2000 SERVICE DISK MANUAL

SOFTWARE VERSION: V5.03

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INTRODUCTION

THIS MANUAL DESCRIBES THE OPERATION AND USE OF THE MCS-2000 "SERVICE DISK", (V5.0 OR HIGHER).

THIS SERVICE DISK IS A SEPARATE DISK WHICH IS COMPATIBLE WITH THE MCS-2000 SYSTEM SOFTWARE VERSION: V5.0 AND IS INTENDED TO BE USED FOR THE CONFIGURATION, CALIBRATION AND FIELD TESTING OF THE MCS-2000.

FUNCTIONAL DESCRIPTION

THE FOLLOWING IS A DESCRIPTION OF ALL FUNCTIONAL CHANGES OF THE SERVICE SOFTWARE FOR THIS VERSION (V5.0):

THE SERVICE PROGRAMME IS COMPATIBLE WITH SYSTEM (V5.0)

THE NEW TESTS ARE, "KEYBOARD" AND THE "NEW KEYPAD". THESE TESTS ARE ADDED TO THE "DIGITAL I/O MENU".

NOTE: THE TEST FOR THE "STANDARD KEYPAD" HAS BEEN RENAMED TO THE "OLD KEYPAD TEST".

THE DIGITAL KV BOARD TEST NOW DISPLAYS THE CHOSEN NUMBER OF CYLINDERS AND THE CORRECT FIRING ORDER IS SELECTED IN THE "SIMULATOR CONFIGURATION" PAGE.

NEW E-EPROM ENTRIES ADDED:

1: PEF ENTRY
2: OIML APPROVAL
3: EXTENDED CRT DRIVER
4: BOLD CHARACTER SET
5: THREE CONFIGURATION OPTIONS
6: EIGHT DEFINITIONS RESERVED FOR FUTURE USE

WHEN THE FACTORY TEST IS SELECTED THE "SIMULATOR CONFIGURATION" PAGE MUST BE ENTERED.

NEW ENTRIES ARE ADDED TO THE "TESTER CONFIGURATION" PAGES AND THE "OPTION ENTRY" PAGES.

NOTE: IT IS POSSIBLE TO PRINT A SCREEN AT ANY STAGE OF TESTING.

OPERATION

1: PLUG THE TESTER INTO THE NEAREST MAINS OUTLET.

2: INSERT THE SERVICE DISK INTO THE DISK DRIVE. SWITCH ON THE POWER TO THE UNIT.

THE TESTER SHOULD PERFORM THE MEMORY TEST ROUTINE, PROGRAMME LOADING SEQUENCE, AFTER THE TESTER CONFIGURATION AND CALIBRATION PAGES HAVE BEEN DISPLAYED, THE "MAIN MENU" PAGE WILL BE DISPLAYED:

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THE MAIN MENU

PROGRAMME SELECTION
- TESTER CONFIGURATION ENTRY
- TESTER CALIBRATION
- GAS BENCH SPECIAL FUNCTIONS
- SPECIAL FUNCTIONS
- LANGUAGE SELECTION
- VEHICLE QUICK TESTS
- FACTORY TESTS

WITH REFERENCE TO THE SERVICE DISK FLOW DIAGRAM, EACH MAIN MENU SELECTION IS DIVIDED INTO A NUMBER OF SUB-MENUS:

1: "TESTER CONFIGURATION ENTRY"
- A: 2 PAGES OF TESTER CONFIGURATION
- B: 2 PAGES OF OPTIONS ENTRY

2: "TESTER CALIBRATION"
- A; 15-MINUTE WARM-UP
- B: TESTER CALIBRATION

3: "GAS BENCH SPECIAL FUNCTIONS"
- A: GAS CALIBRATION
- B: MODULE DISPLAY
- c: GAS ANALYSER CHECK
- D: ALTITUDE ENTRY
- E: PEF ENTRY

DEPENDING ON GAS BENCH CONFIGURATION

4: "SPECIAL FUNCTIONS"
- A: CUSTOMER MESSAGE EDITOR
- B: DATE AND TIME ENTRY
- c: SCREEN SAVER FUNCTION

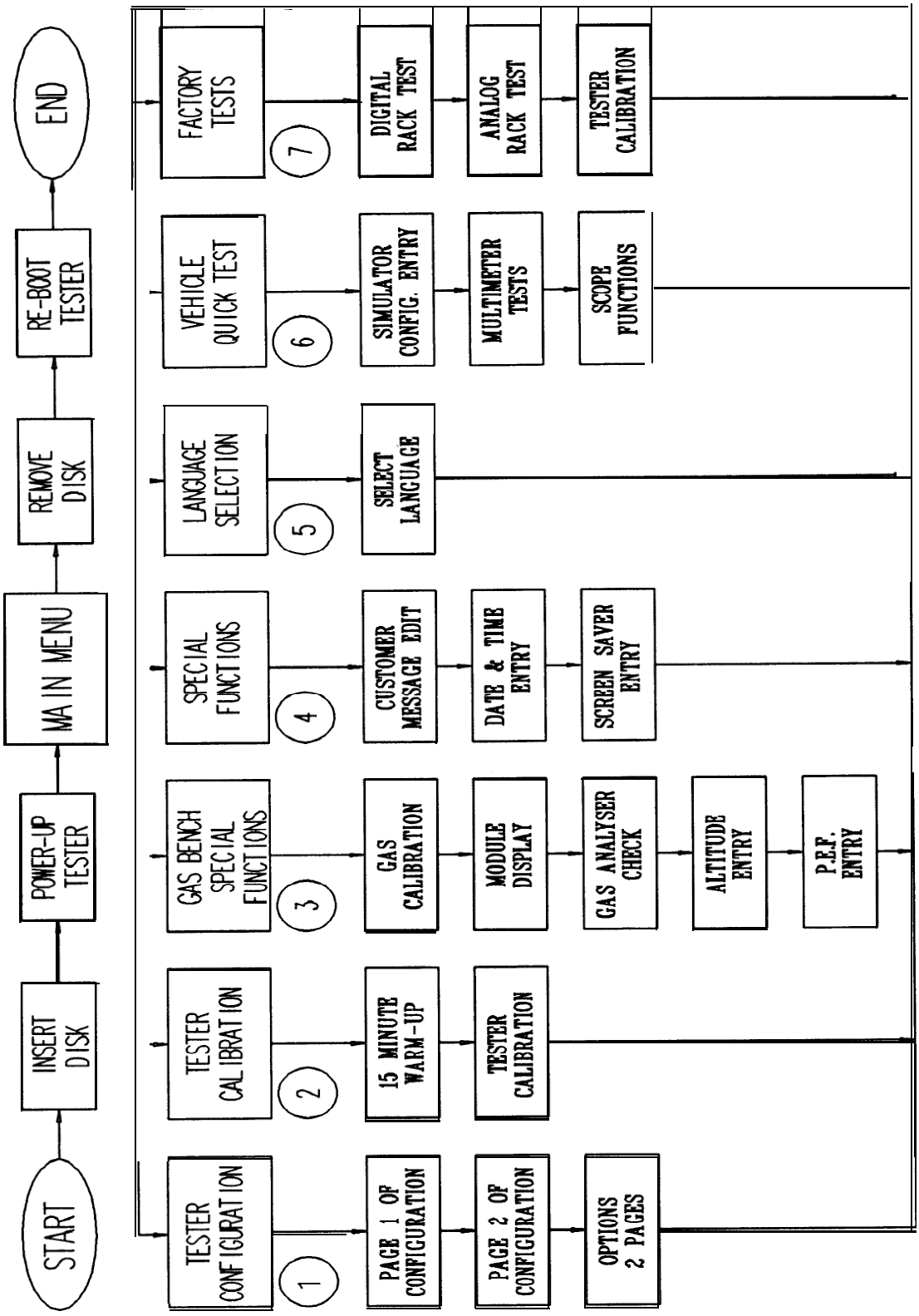
5: "LANGUAGE SELECTION"
- A: SELECT SYSTEM LANGUAGE

6: "VEHICLE QUICK TEST"
- A: SIMULATOR CONFIGURATION ENTRY
- B: MULTIMETER TESTS
- c: SCOPE FUNCTIONS

7: "FACTORY TESTS"
- A: DIGITAL RACK TESTS
- B: ANALOG RACK TESTS
- c: TESTER CALIBRATION

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MCS-2000 SERVICE DISK FLOW DIAGRAM



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A: TESTER CONFIGURATION ENTRY

THE TESTER CONFIGURATION MENU CONSISTS OF TWO PAGES. THESE PAGES CONTAIN A NUMBER OF ITEMS THAT CAN BE SET TO "DEFINED" OR "NOT DEFINED" DEPENDING ON THE CONFIGURATION OF THE TESTER. THE CONFIGURATION DEFINITIONS WILL BE SAVED INTO THE E-EPROM MEMORY WHEN THESE PAGES ARE EXITED.

TESTER CONFIGURATION ENTRY, PAGE 1:

TESTER CONFIGURATION ENTRY	
- DIESEL OPTION	NOT DEFINED
- DIAGNOSTICS	NOT DEFINED
- TECH-15	NOT DEFINED
- DIGITAL SCOPE	DEFINED
- BAROMETER	DEFINED
- KEYBOARD	NOT DEFINED
- DATE AND TIME	NOT DEFINED
- SDL-20	DEFINED
- OIML	NOT DEFINED

STEP THROUGH ALL LINES BY SETTING "DEFINED/NOT DEFINED" AS REQUIRED, BY PRESSING THE # KEY. WHEN THE # KEY IS PRESSED ON THE LAST LINE, THE CAPTION "WRITING TO MEMORY" WILL BE DISPLAYED.

TESTER CONFIGURATION ENTRY, PAGE 2:

THE DEFINITIONS "BIT 13, BIT 14 & BIT 15" ARE INTENDED FOR FUTURE USE AN SHOULD BE LEFT AS "NOT DEFINED".

TESTER CONFIGURATION ENTRY	
- EXT. CRT DRIVER	NOT DEFINED
- BIT 13	NOT DEFINED
- BIT 14	NOT DEFINED
- BIT 15	NOT DEFINED

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B: OPTIONS ENTRY

THE OPTIONS ENTRY ALSO CONSISTS OF TWO PAGES. THESE PAGES PROVIDE THE ABILITY TO CONFIGURE THE TESTER ACCORDING TO THE OPTIONS INSTALLED.

OPTIONS ENTRY, PAGE 1:

TESTER OPTIONS ENTRY	
- KEYPAD TYPE	STANDARD
- PRINTER TYPE	OKI-182E
- GAS BENCH TYPE	SGM-2004
- GASES AVAILABLE	HC/CO2/CO
- GAS APPROVAL	PTB
- COUNTRY CODE	GERMANY

OPTIONS ENTRY, PAGE 2:

THIS PAGE IS RESERVED FOR FUTURE USE. EACH ENTRY CAN BE DEFINED AS A DECIMAL VALUE FROM 0 TO 255.

TESTER OPTIONS ENTRY	
- ADDRESS 403223	000
- ADDRESS 403225	000
- ADDRESS 403227	000
- ADDRESS 403229	000
- ADDRESS 40322A	255
- ADDRESS 403226	000
- ADDRESS 40322E	000
- ADDRESS 403231	000

NOTE: RE-BOOT THE TESTER WHEN CHANGES ARE MADE TO THE TESTER CONFIGURATION PAGES.

****

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2: TESTER CALIBRATION

A: THE 15-MINUTE WARM UP

WHEN THE TESTER CALIBRATION IS SELECTED FROM THE MAIN MENU, THE TWO (2) TESTER CONFIGURATION PAGES WILL BE DISPLAYED FOLLOWED BY A 15 MINUTE WARM-UP PERIOD. (PRESS " * " TO OVER-RIDE THE WARM-UP).

B: TESTER CALIBRATION

WHEN THE 15 MINUTE WARM-UP IS COMPLETED THE TESTER CALIBRATION WILL START.

TESTER CALIBRATION	
- ADC REFERENCE	PASS
- AMPS	PASS
- RIPPLE	PASS
- ANALOG KV	PASS
- VOLT/OHM	PASS
- VACUUM	PASS
- HC	PASS
- co	PASS
- co2	PASS
- 02	PASS
- BPC	PASS

THIS PAGE WILL BE DISPLAYED AFTER ANY OF THE FOLLOWING:

AUTOMATICALLY WHEN THE TESTER IS FIRST POWERED UP.

WHEN THE "GAS BENCH SPECIAL FUNCTIONS", "GAS CALIBRATION" IS SELECTED.

WHEN THE "ANALOG RACK TEST", "TESTER CALIBRATION" IS SELECTED.

IF A CALIBRATION ERROR HAS OCCURRED THE MESSAGE "CALIBRATION FAILURE" WILL BE DISPLAYED ON THE LAST LINE OF THE SCREEN, WHEN THE TESTER CALIBRATION HAS BEEN SUCCESSFUL THE MAIN MENU PAGE WILL BE DISPLAYED.

****

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GAS BENCH SPECIAL FUNCTIONS
- GAS CALIBRATION
- MODULE DISPLAY

THE MENU LAYOUT OF THIS FUNCTION IS DEPENDANT ON THE CONFIGURATION OF THE TESTER. THE POSSIBLE MENU ITEMS ARE AS FOLLOWS:

1: WHEN THE "GAS APPROVAL" TYPE IS DEFINED AS "APK", THEN THE "APK GAS ANALYSER CHECK" IS ADDED TO THIS MENU.

2: WHEN THE "GAS APPROVAL" TYPE IS DEFINED AS "PTB", THEN THE "PTB GAS ANALYSER CHECK" IS ADDED TO THIS MENU.

3: WHEN THE "BAROMETER" OPTION IS NOT INSTALLED AND THE GAS APPROVAL TYPE IS NOT DEFINED AS "APK", THEN THE "ALTITUDE ENTRY" IS ADDED TO THIS MENU.

4: WHEN THE "OIML" IS DEFINED AND THE SELECTED GAS BENCH IS THE "SGM-2004", THEN THE PROPANE EQUIVALENCY FACTOR "PEF" IS ADDED TO THIS MENU.

A: GAS CALIBRATION:

DEPENDING ON THE DEFINITION OF THE BAROMETER CONFIGURATION, ONE OF TWO DIFFERENT PAGES IS ENTERED:

ALTITUDE ENTRY

BAROMETRIC PRESSURE DISPLAY

ALTITUDE ENTRY

THE FIRST PAGE, ENTERED WHEN "BAROMETER" IS "NOT DEFINED" PROVIDES THE USER WITH THE POSSIBILITY TO SET THE LOCAL ALTITUDE (0 TO 5000 M) BEFORE ENTERING THE GAS CALIBRATION PAGE.

ALTITUDE ENTRY
- ALTITUDE (M) : ....

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BAROMETRIC PRESSURE DISPLAY

WHEN THE "BAROMETER" OPTION IS "DEFINED", THEN CALIBRATION OF THE BAROMETER CAN BE PERFORMED. THIS PAGE ENABLES THE USER TO CORRECT THE OUTPUT VOLTAGE FROM THE PRESSURE TRANSDUCER AND THE IMMEDIATE CALCULATED PRESSURE IS ALSO DISPLAYED.

BPC CALIBRATION	
- BAROMETER (VOLT):	. ....
- PRESSURE (MBAR):	....

AFTER PROCEEDING THROUGH THE PREVIOUS PAGE, THE GAS CALIBRATION PAGE IS ENTERED. IN THIS PAGE IT IS POSSIBLE TO PERFORM A HARDWARE GAS CALIBRATION.

BY FOLLOWING THE INSTRUCTIONS GIVEN ON THE MONITOR THE HARDWARE CAN BE CALIBRATED.

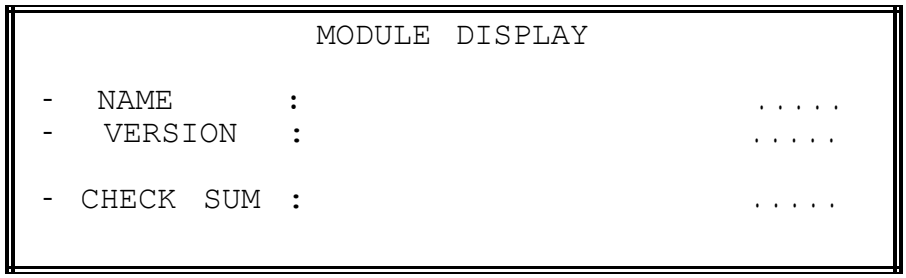
GAS CALIBRATION

	ZERO VOLTAGE	GAS VALUES	SPAN VOLTAGE
CO	.....	.... %	.....
HC	.....	.... PPM	.....
CO2	.....	.... %	.....
02	.....	.... %	.....

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B: MODULE DISPLAY

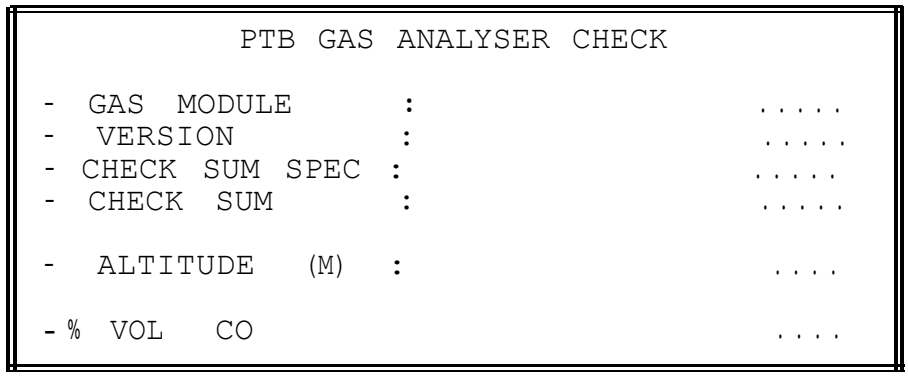
THE MODULE DISPLAY SHOWS A NUMBER OF CHARACTERISTICS OF THE GAS MODULE INSTALLED. THE NAME AND VERSION NUMBER ARE DERIVED DIRECTLY FROM THE GAS BENCH SOFTWARE.
THE CHECKSUM DISPLAYED IS (HARD)CODED INTO THE SOFTWARE. THIS CHECKSUM IS ALWAYS THE SAME FOR A CERTAIN RELEASED VERSION OF A PARTICULAR GAS BENCH.



C: GAS ANALYSER CHECKS

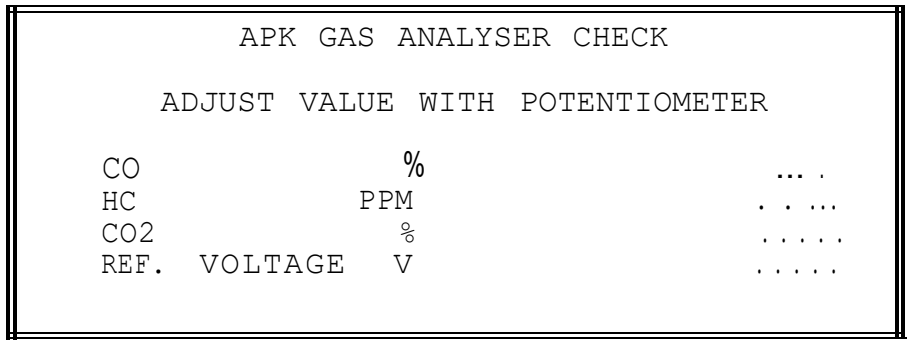
THE PAGE LAYOUT OF THIS FUNCTION IS DEPENDANT ON THE CONFIGURATION OF THE TESTER. THE FOLLOWING SHOW THE POSSIBLE PAGES:

PTB GAS ANALYSER CHECK



APK GAS ANALYSER CHECK

WHEN AN ANDROS (SGM-2004) GAS BENCH IS INSTALLED, THE APK GAS ANALYSER CHECK IS DIFFERENT WHEN ANOTHER GAS BENCH IS INSTALLED.



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PAGE LAYOUT FOR APK GAS ANALYSER CHECK WITH AN ANDROS GAS BENCH.

APK WITH ANDROS BENCH		
ADJUST VALUE WITH POTENTIOMETER		
CO ZERO	V	.....
CO	%	.....

****

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4: SPECIAL FUNCTIONS

```
SPECIAL FUNCTIONS

- CUSTOMER MESSAGE EDITOR

- DATE AND TIME ENTRY

- SCREEN SAVER ENTRY
```

A: CUSTOMER MESSAGE EDITOR

IN THIS PAGE, A MESSAGE CAN BE ENTERED ON TO THE SCREEN. THIS MESSAGE WILL BE SAVED INTO E-EPROM MEMORY AND CAN BE RETRIEVED AND PRINTED AT A LATER STAGE.

B: DATE AND TIME ENTRY

THE REAL TIME CLOCK KIT MUST BE INSTALLED AND DEFINED IN ORDER TO ENTER THE DATE AND TIME.

```
DATE & TIME ENTRY

ENTER TIME (HH:MM:SS)        .. : .. : ..

ENTER DATE (DD/MM/YY)        .. / .. / ..
```

C: SCREEN SAVER ENTRY

```
MCS-2000 VERSION: 5.0

TIMEOUT  :                          ...

RANGE    : 0 TO 255 MINUTES

A ZERO VALUE TURNS SCREEN SAVER OFF.

RE-BOOT TESTER TO MAKE NEW TIMEOUT ACTIVE
```

****

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5: LANGUAGE SELECTION

THIS PAGE IS USED TO SELECT ANOTHER LANGUAGE. WHEN ANOTHER LANGUAGE IS AVAILABLE, THIS PAGE ALLOWS THE USER TO SELECT ANOTHER LANGUAGE (OR THE ONE THAT IS CURRENTLY IN USE) AND LOADS IT INTO MEMORY. AFTER THIS ALL TEXT WILL BE DISPLAYED IN THE NEW LANGUAGE.

****

6: VEHICLE QUICK TEST

THESE PAGES LEAD THE USER THROUGH THE "SIMULATOR CONFIGURATION" ENTRY SCREENS AND GIVE THE ABILITY TO CONFIGURE A TYPE OF ENGINE FOR SEVERAL TESTS.

SIMULATOR CONFIGURATION

ENGINE TYPE:	LPG
NUMBER OF CYLINDERS:	4
FIRING ORDER:	1- 3- 4- 2
CYLINDER STROKE:	4
MAG PROBE:	YES
TDC OFFSET:	-20.0

THE NEXT PAGE THAT IS ENTERED IS DEPENDENT ON WETHER THE DIGITAL SCOPE IS DEFINED OR NOT DEFINED.
IF DEFINED, THE NEXT PAGE SHOWS THE FOLLOWING OPTIONS:

VEHICLE QUICK TEST

- MULTIMETER TESTS
- SCOPE FUNCTIONS

OTHERWISE THE FIRST OPTION, "MULTIMETER TESTS" ARE ENTERED DIRECTLY.

A: MULTIMETER TESTS

THE "MULTIMETER TEST PAGES" ARE IDENTICAL TO THE PAGES THAT ARE ON THE MCS-2000 SYSTEM DISK.

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MULTIMETER TEST 1

```
                MULTIMETER TEST 1

ENGINE                    RPM          .....
BATTERY                 VOLTS          .....
ALT. RIPPLE               %            .....
CURRENT                  AMPS          .......
COIL +/KL.15            VOLTS          ......
COIL -/KL.1             VOLTS          .....
DWELL                                  .....
PEAK  FIRING  VOLTAGE   KV             .....
HC                       PPM           .....
OIL TEMPERATURE          OC            .....
```

MULTIMETER TEST 2

```
          MULTIMETER TEST 2 (PAGE 1)

ENGINE                    RPM          .....
TIMING                                 .....
DWELL                                  .....
PEAK  FIRING  VOLTAGE   KV             .....
VACUUM                  MBAR           .....
OIL TEMPERATURE           °C           .....
```

SECONDARY PAGE LAYOUT

```
          MULTIMETER TEST 2 (PAGE 2)

ENGINE                    RPM          .....
CO                          %          .....
HC                        PPM          .....
CO2                         %          .....
02                          %          . ....
LAMBDA CALCULATED                      .....
AIR FUEL RATIO                         .....
OIL TEMPERATURE           °C           .....
```

MULTIMETER TEST 3

```
                MULTIMETER TEST 3

METER VOLTAGE           VOLTS          .....

RESISTANCE               OHMS          ......
```

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B: SCOPE FUNCTIONS

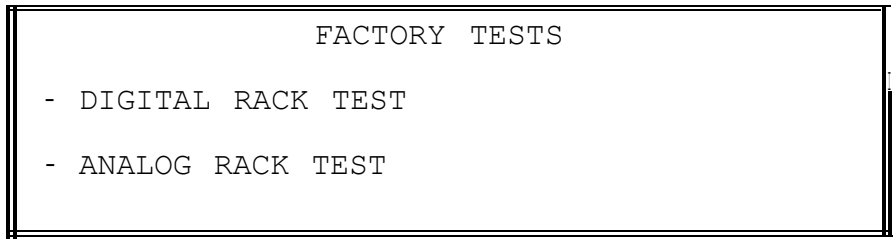
THE SCOPE FUNCTIONS ARE IDENTICAL TO THOSE ON THE MCS SYSTEM DISK.

****

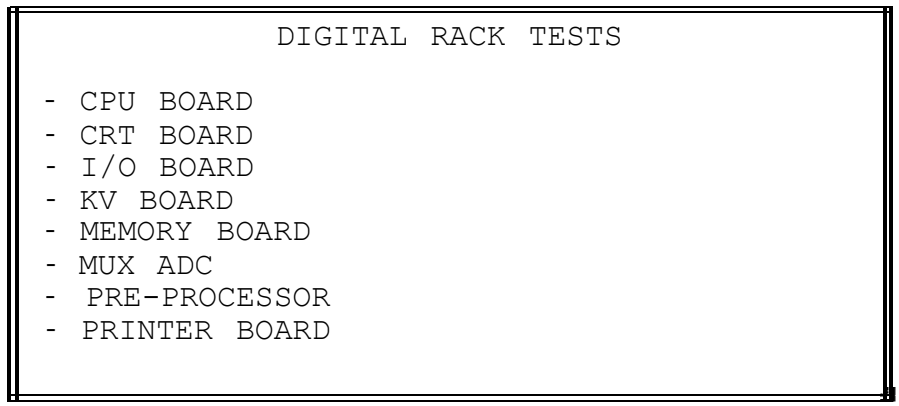
7: FACTORY TESTS

BEFORE THE FACTORY TEST MENU APPEARS THE "SIMULATOR CONFIGURATION" ENTRY MUST BE ENTERED. THE "FACTORY TEST" MENU IS DIVIDED INTO TWO MAIN CATEGORIES:

A: TESTS ALL DIGITAL FUNCTIONS OF THE TESTER.
B: TEST THE ANALOG CIRCUITRY OF THE TESTER.

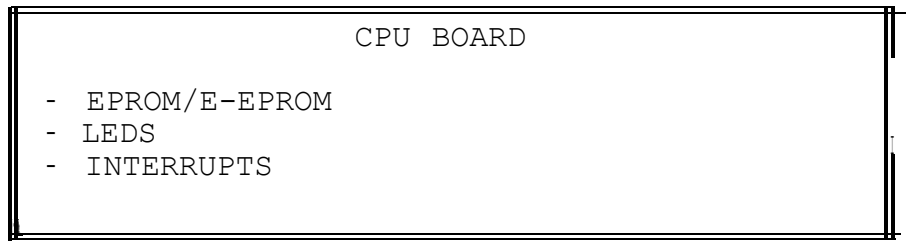


A: DIGITAL RACK TESTS



A.1: CPU BOARD

THE CPU BOARD TEST CONTAINS THREE ENTRIES. EACH SERVES TO MONITOR THE FUNCTIONING OF A SPECIFIC PART OF THE BOARD.



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EPROM/E-EPROM TEST

THIS PAGE SHOWS THE CHECKSUMS OF THE EPROM AND THE E-EPROM. THE CHECKSUMS INDICATE IF THE INFORMATION CONTAINED IN THE RESPECTIVE PROMS IS RELIABLE.

FOR THE EPROM THE LEAST SIGNIFICANT BYTE SHOULD ALWAYS BE 0x55H.

```
              EPROM / E-EPROM TEST

CHECKSUMS:                  CALC:     SPEC:

EPROM:
 LOW BYTE  (E4)             ....      xx55
 HIGH BYTE (E2)             ....      xx55

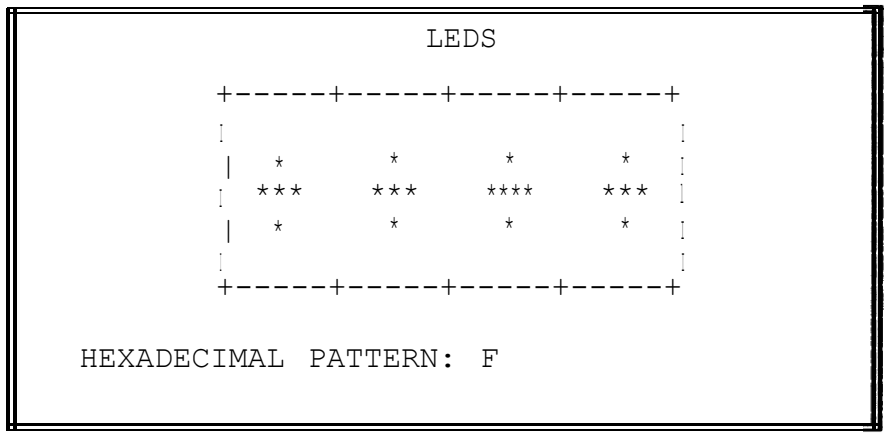
E-EPROM:
 LOW BYTE  (F4)             ....      ----
 HIGH BYTE (F2)             ....      ....
```

LEGEND: **XX** = NO SPECIFICATION

--- = SPECIFICATION NOT POSSIBLE BECAUSE LOW BYTE IS NOT USED IN THIS CONFIGURATION.

LEDS TEST

THE LED TEST ENABLES THE USER TO INDIVIDUALLY ACTIVATE ANY OF THE FOUR LEDS ON THE CPU BOARD. BY STEPPING THROUGH THE VARIOUS INPUT VALUES, A DIFFERENT PATTERN IS DISPLAYED. THIS PATTERN IS FROM LEFT TO RIGHT THE HEXADECIMAL VALUE THAT IS ENTERED. (LED ON = 1).

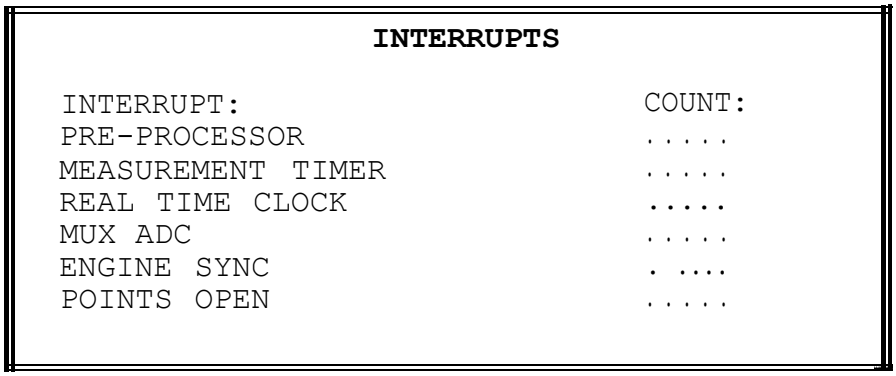


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INTERRUPTS

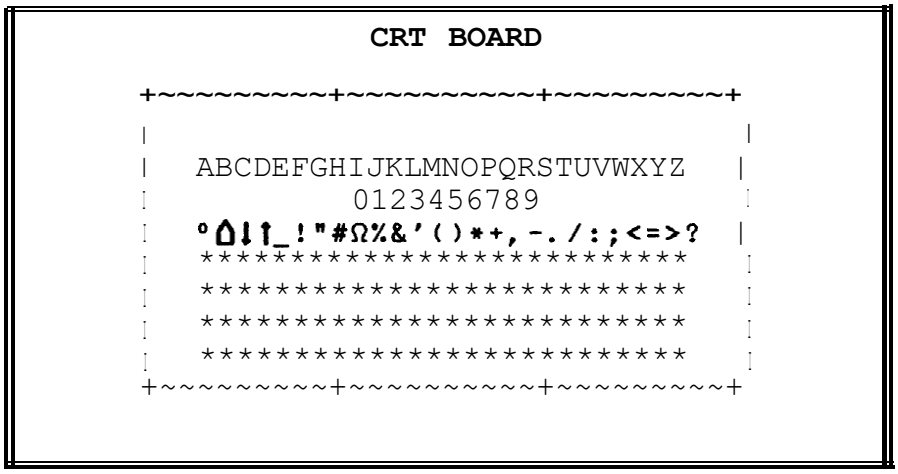
THE INTERRUPTS TEST CONTINUOUSLY DISPLAYS A NUMBER OF COUNTERS. EACH COUNTER SHOWS THE TOTAL NUMBER OF INTERRUPTS THAT THE CPU RECEIVED SINCE THE TEST PAGE WAS ENTERED. WHILE IN THE TEST PAGE THE COUNTERS ARE CONTINUOUSLY UPDATED.

EACH OF THE COUNTERS DISPLAYS THE NUMBER OF INTERRUPTS THAT A SPECIFIC HARDWARE DEVICE GENERATES.



A.2: CRT BOARD TEST

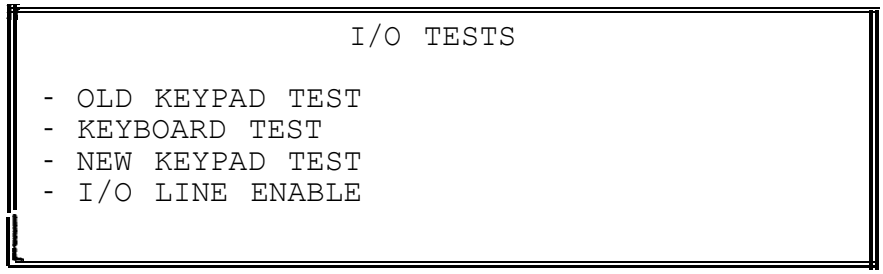
THE CATHODE RAY TUBE TEST IS DESIGNED TO TEST THE CRT RAM. THE RAM IS TESTED BY WRITING A VALUE TO RAM AND SUBSEQUENTLY READ THAT RAM LOCATION. WHENEVER DIFFERENT VALUES ARE FOUND, A CRT FAILURE MESSAGE WILL BE DISPLAYED.



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A.3: I/O TESTS

THE DIGITAL I/O TEST CONTAINS TESTS THAT COMMUNICATE THROUGH THE DIGITAL I/O PORTS. THESE PORTS/LINES CAN BE TESTED DIRECTLY.



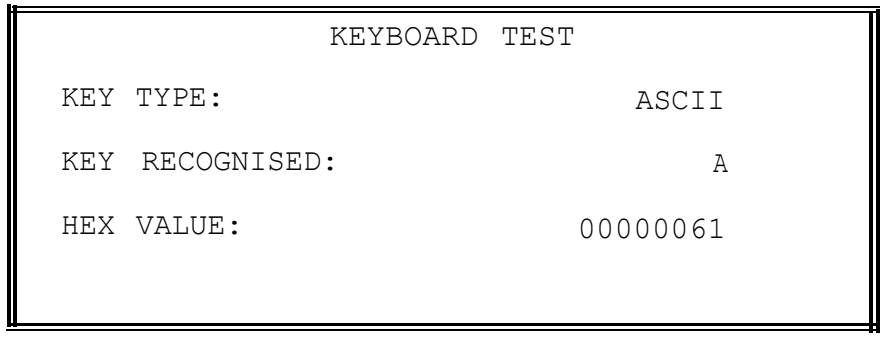
OLD KEYPAD TEST

THE DISPLAY CONTAINS THE LAYOUT OF THE STANDARD MCS-2000 KEYPAD. BY PRESSING A KEY ON THE KEYPAD (EXCEPT FOR "P"), THE ACTUAL FUNCTIONING OF THE KEY CAN BE CHECKED.

KEYBOARD TEST

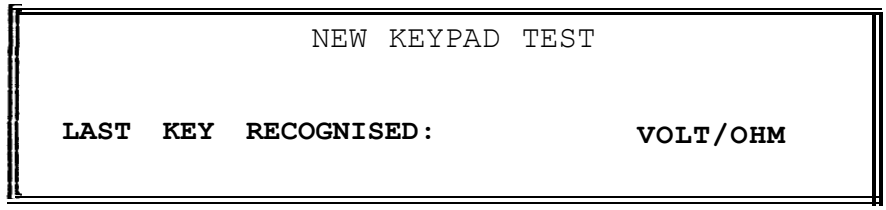
WHEN A KEY ON THE KEYBOARD IS PRESSED THE DISPLAY IS UPDATED. SOME KEYBOARD FUNCTIONS HAVE THE SAME FUNCTION AS A KEYPAD KEY.

IF THE DETECTED KEY IS OF THE KEYPAD TYPE, THEN THE DISPLAY IS THE EQUIVALENT KEYPAD KEY; THE HEX VALUE WILL BE CLEARED.



NEW KEYPAD TEST

THE KEYPAD KEY PRESSED CAUSES THE TEST TO DISPLAY A TEXT SCREEN THAT CORRESPONDS TO THE FUNCTION OF THAT KEY.



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I/O LINE ENABLE

TEST DIGITAL I/O LINES. THE LINE CAN BE TESTED BY SETTING A "1" OR A "0" ON THE OUTPUT. (RELAYS AND SOLENOIDS CAN BE HEARD ACTIVATING).

I/O LINE ENABLE	
SHORT CYLINDER:	OFF
GAS SPAN RELAY:	OFF
GAS PURGE RELAY:	ON
OHMS RANGE RELAY:	OFF
VOLT/OHM SELECT:	ON
PRIMARY ENABLE:	OFF
AMPS RANGE SELECT:	OFF
ENGINE KILL:	OFF

A.4: DIGITAL KV BOARD

MEASUREMENTS OF INTERVAL (DWELL) AFTER CYLINDER FIRING FOR EACH CYLINDER. THE NUMBER OF CYLINDERS AND THE FIRING ORDER WAS SELECTED BEFORE ENTERING THE FACTORY TEST IN THE SIMULATOR CONFIGURATION PAGE.

KV BOARD		
CYL #	MSEC	DUR
1	....	...
3	.....	...
2	....	...
4	....	...

A.5: MEMORY BOARD

THE SYSTEM RAM CHIPS CAN BE TESTED IN THIS PAGE.

MEMORY BOARD		
SOCKETS	ADDRESS	STATUS
H1/H2	10000	.....
G1/G2	30000	
F1/F2	50000	::::::
E1/E2	70000	.....
D1/D2	90000	.....
C1/C2	B0000	
B1/B2	D0000	::::::
A1/A2	F0000	.....

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THE STATUS CAN BE ONE OF THE FOLLOWING:

- TESTING	:	BUSY TESTING THE RAM SOCKET
- GOOD	:	RAM SOCKET TEST SUCCESSFUL
- INCOMPLETE	:	TESTING RAM SOCKET SKIPPED BY PRESSING *#*
- ****: ****:****	:	FAILURE DETECTED AT THIS ADDRESS.

A.6: MUX ADC BOARD

TEST ZERO (0) AND SPAN (2000) OF RANGES 1.835 AND 7.350 VOLTS EACH.

MUX ADC BOARD

GAIN	REF	COUNTS	ADJUST TO
Xl	ZERO	. . . . .	VOLTS
X1	SPAN	. . . . .	VOLTS
x4	ZERO	. . . . .	VOLTS
x4	SPAN	. . . . .	VOLTS

CONVERSION TIME: . . . . . US

A.7: PRE-PROCESSOR BOARD

THREE SELECTIONS CAN BE MADE IN THE PRE-PROCESSOR BOARD TEST.

PRE-PROCESSOR BOARD

- PRE-PROCESSOR STATUS
- PRE-PROCESSOR READINGS
- SHORT CYLINDER TEST

PRE-PROCESSOR STATUS

IN THIS PAGE THE STATUS OF THE PRE-PROCESSOR IS DISPLAYED.

PRE-PROCESSOR STATUS

ENGINE SYNCHRONISATION	:	ON
MAGNITUDE SIGNAL	:	OFF
CYLINDER CLOCK	:	ON

NUMBER OF CYLINDERS DETECTED: 4

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PRE-PROCESSOR READINGS

THIS PAGE DISPLAYS THE CURRENT READINGS OF THE PRE-PROCESSOR.

PRE-PROCESSOR READINGS			
AVERAGE RPM	:	...	RPM
INSTANT RPM	:	...	RPM
AVERAGE DWELL	...	%	
INSTANT DWELL	...	%	
AVERAGE TIMING	:	...	°
INSTANT TIMING	:	...	°

SHORT CYLINDER TEST

ENTER CYLINDER NUMBERS IN FIRING ORDER. THE CYLINDER SELECTED WILL BE INSTANTLY SHORTED.

SHORT CYLINDER TEST		
CYLINDER NUMBER	:	4

A.8: PRINTER BOARD

TEST PRINTER BOARD. PRESSING THE PRINT KEY WHEN IN THIS PAGE WILL SEND ALL CHARACTERS FROM THE DISPLAY MEMORY TO THE PRINTER.

B: ANALOG RACK TEST

SECOND SUB-MENU OF FACTORY TESTING. THIS PAGE SHOWS THE POSSIBLE ENTRIES OF PAGES THAT LEAD TO VARIOUS TESTS OF ANALOG PARTS OF THE TESTER.

ANALOG RACK TEST
- AMPS BOARD
- VOLT/OHM BOARD
- PEAK KV/RIPPLE
- SPARK KV/SLOPE
- BOOM POD
- TESTER CALIBRATION

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B.1: AMPS BOARD

SELECT AMPS 100 OR AMPS 1K RANGE AND TEST MUX VOLTAGE. THE VALUES READ ARE DISPLAYED IN TWO FORMATS; A RAW VALUE READ DIRECTLY AND AN AVERAGE VALUE.

```
                AMPS BOARD

                VALUE                  MUX
                                     VOLTAGE
AMPS 100 ZERO                         .....
AMPS  1K ZERO                         .......

AVERAGE AMPS    .....
AMPS RANGE      .....
```

B.2: VOLT/OHM BOARD

SELECT MVOLT OR OHMS AND TEST MUX VOLTAGE.

```
                VOLT/OHM BOARD

                 VALUE     MUX       VOLTAGE
                           ZERO         READ
VOLTS    V          ...    ....       .......
OHMS     Ω                             .......
OHMS OPEN                              .......
OHMS SPAN                              .......
OHMS ZERO                              .......

MEASUREMENT TYPE          . ...
```

B.3: PEAK KV/RIPPLE

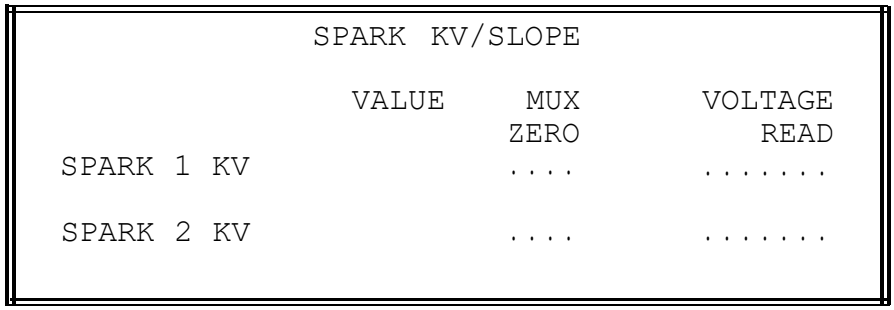
TEST MUX VOLTAGES FOR THE PEAK KV TEST.

```
                PEAK KV/RIPPLE

                 VALUE     MUX       VOLTAGE
                           ZERO         READ
PKKV    KV         ...     ....       .......
RIPPLE   V       .....     ....       .......
         %         ...     ....       .......
BATTERY V          ...                .......
```

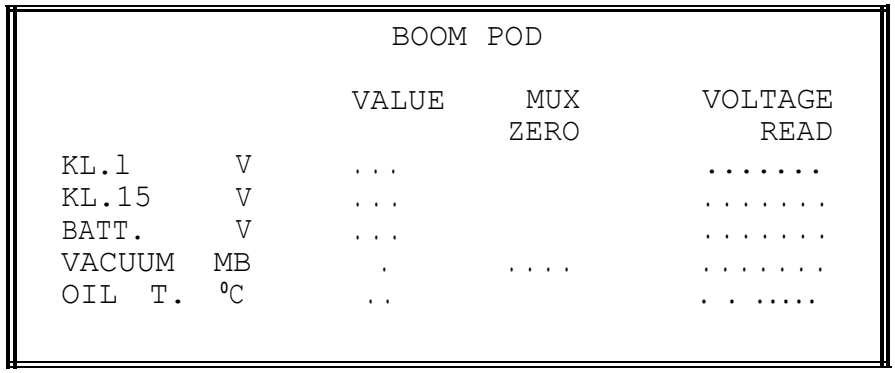

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B.4: SPARK KV/SLOPE



B. 5: BOOM POD TEST

TEST THE BOOM POD. THE VALUES ARE READ FROM THE INPUTS AND DISPLAYED DIRECTLY 0N THE SCREEN.



B.6: TESTER CALIBRATION

THIS PAGE IS IDENTICAL TO THE "TESTER CALIBRATION" FUNCTION IN THE MAIN MENU AND TO LAST PAGE OF THE "GAS BENCH SPECIAL FUNCTIONS" MENU.

****

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SYSTEM ERROR CODES:

2 - NO SUN DISKETTE

MONITOR ERROR CODES:

100 - INVALID COMMAND
101 - INVALID TERMINATOR (COMMA OR CARRIAGE RETURN EXPECTED)
102 - INVALID CHARACTER (OTHER CHARACTER EXPECTED)
103 - ODD ADDRESS (CAN NOT JUMP TO AN ODD ADDRESS)
104 - INVALID INPUT DEVICE
105 - INVALID OUTPUT DEVICE
109 - EPROM VERIFY
110 - BAD ADDRESS

FTU/KEYBOARD COMMAND ERRORS ONLY APPLICABLE WHILST IN THE SERVICE PROGRAM.

FLOPPY DISC CONTROLLER ERROR CODES:

81 - INCORRECT PARAMETER PASSED TO FDC ROUTINE (PROGRAM ERROR)
82 - TRACK 00 BIT NOT SET IN STATUS REG.(RESTORE)(DRIVE OR FDC ERR.)
83 - SPIN UP ERROR, NOT 6 SPIN UP REVS.DETECTED (DRIVE OR FDC ERR.)
84 - CRC ERROR IN ID FIELD (DISC OR DRIVE ERR.)
85 - CRC ERROR IN DATA (DISC OR DRIVE ERROR)
86 - TRACK NUMBER VERIFY ERROR (DISC OR DRIVE ERR.)
87 - BUSY BIT ALWAYS SET (FDC ERR.)
88 - BUSY BIT ALWAYS RESET (FDC ERR.)
89 - LOST DATA BIT SET (READ/WRITE) (FDC ERR.)
90 - OISK WRITE PROTECTED (DISC, DRIVE OR FDC ERR.)
91 - RECORD NOT FOUND (DISC, DRIVE OR FDC ERR.)
93 - END OF MEDIA (LAST TRACK PASSED) (DRIVE OR FDC ERR.)
95 - WRONG BYTE COUNT RETURNED (READ/WRITE) (DISC, DRIVE OR FDC ERR.)
96 - PATTERN ERROR ON TEST TRACKS (DISC OR DRIVE ERR.)
97 - INCORRECT ID READ (DISC OR DRIVE ERR.)

SEE TROUBLE SHOOTING FOR DISC ERRORS.

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INTERRUPT ERROR CODES:

0 - BUS ERROR
1 - ADDRESS ERROR
2 - ILLEGAL INSTRUCTION
3 - ZERO DIVIDE ERROR
4 - CHECK INSTRUCTION
5 - TRAP INSTRUCTION
6 - PRIVILEGED INSTRUCTION
7 - TRACE INSTRUCTION
8 - A-LINE INTERRUPT
9 - F-LINE INTERRUPT
10 - UNINITIALIZED INTERRUPT
11 - SPURIOUS INTERRUPT
12 - AUTO VECTOR INTERRUPT
13 - USER TRAP INTERRUPT
14 - RESERVED EXCEPTION
15 - USER VECTOR EXCEPTION

DIGITAL RACK OR POWER SUPPLY ERRORS.

SEE TROUBLE SHOOTING

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1. SET-UP 2.4

THE MCS 2000 HAS VARIOUS MODES OF OPERATION DEPENDING UPON CONDITIONS AND OPTIONS INSTALLED. TO ENSURE YOUR TESTER IS SET-UP CORRECTLY THE FOLLOWING INSTRUCTIONS SHOULD BE FOLLOWED BEFORE ANY CHECK-OUT OR CALIBRATION 'PROCEDURES ARE MADE.

IMPORTANT

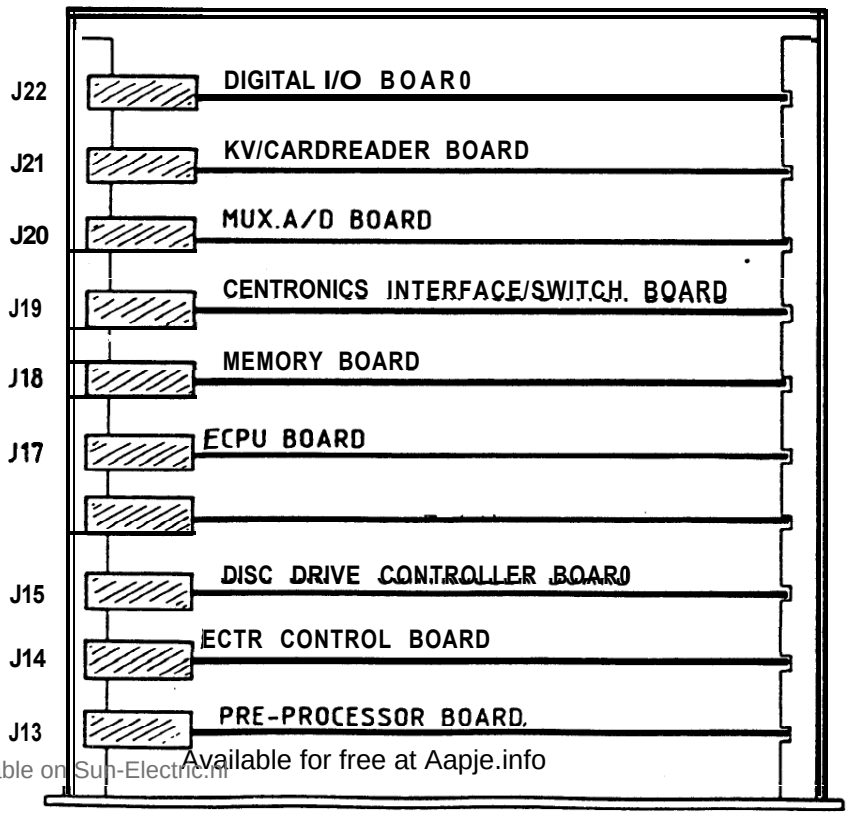
IF THE TESTER IS INCORRECTLY SET-UP SOME FUNCTIONS MAY APPEAR TO MALFUNCTION. DO NOT CONDEMN A TESTER UNTIL ALL SET-UP PROCEDURES HAVE BEEN CHECKED.

AS THE MCS 2000 IS AVAILABLE WITH A VARIETY OF OPTIONS THIS PROCEDURE COVERS THE BASIC TESTER ONLY EXCLUDING ALL OPTIONS. THEREFORE TO CARRY OUT A FULL SET-UP PROCEDURE INCLUDING ANY OPTION(S) FITTED IT IS IMPORTANT THAT THE RELEVANT SECTION REFERRING TO THE OPTION(S) SHOULD ALSO BE REVIEWED.

THE BASIC TESTER IS SUPPLIED WITH THE FOLLOWING SUB ASSEMBLIES :

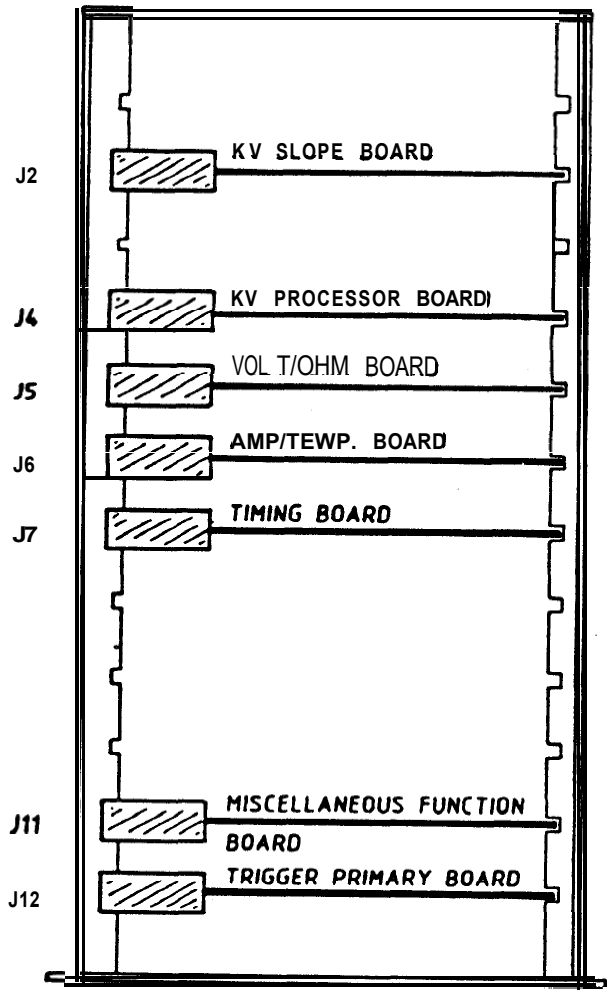
A - VDU ASSY

B - DIGITAL CARD RACK



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C - ANALOG CARD RACK



D - DISC DRIVE ASSEMBLY

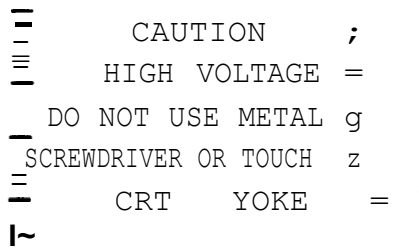
E - POWER SUPPLY 240/220/110V-50/60HZ

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SET-UP

A - VDU ASSY

THE VDU ASSEMBLY IS NORMALLY FACTORY SET HOWEVER SHOULD ADJUSTMENT BE NECESSARY THE FOLLOWING SEQUENCE SHOULD BE FOLLOWED.



CONTRAST:
VR 9 "VIDEO GAIN".
SET VR 9 TO GIVE A NORMAL DISPLAY.

BRIGHTNESS:
VR6 BRIGHTNESS CONTROL.
VR6 SHOULD BE SET TO GIVE DESIRED VIDEO BRIGHTNESS.

V. HOLD:
VERTICAL HOLD, IF THE PICTURE IS ROLLING IN THE VERTICAL DIRECTION, ADJUST VR1.

H. HOLD:
HORIZONTAL HOLD, IF THERE IS NO HORIZONTAL LOCK, ADJUST L2.

H. LIN:
HORIZONTAL LINEARITY, IF THE WIDTH OF THE CHARACTERS AT THE LEFT HAND SIDE OF THE DISPLAY IS NOT EQUAL TO THOSE ON THE RIGHT HAND SIDE, ADJUST L3.

H. AMP:
HORIZONTAL AMPLITUDE, L4 CAN BE ADJUSTED TO GIVE A PICTURE OF THE REQUIRED WIDTH.

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VERTICAL LINEARITY:

VR4 (GEN.LIN.), SHOULD BE ADJUSTED TO EQUALIZE THE HEIGHT OF THE CHARACTERS AT THE TOP OF THE SCREEN WITH THOSE AT THE CENTR.

VR3 (BOTT LIN.), IS THEN SET TO EQUALIZE THE HEIGHT OF THE CHARACTERS AT THE SCREEN BOTTOM WITH THOSE AT THE CENTRE.

V. AMP:

VERTICAL AMPLITUDE (HEIGHT)

VR2 CAN BE ADJUSTED TO GIVE A PICTURE OF THE REQUIRED HEIGHT.

V. SHIFT:

VERTICAL SHIFT. ADJUST VR10 TO POSITION THE DISPLAYED INFORMATION CENTRALLY IN THE VERTICAL AXIS OF THE CRT.

FOCUS:

VR8 IS SET TO GIVE THE BEST OVERALL FOCUS PERFORMANCE WITH THE CONTRAST AND BRIGHTNESS CONTROLS ADJUSTED TO GIVE A NORMAL DISPLAY.

HF ADJUST:

L1 IS ADJUSTED TO EQUALIZE THE INTENSITY OF THE VERTICAL PARTS OF CHARACTERS WITH THAT OF THE HORIZONTAL PARTS.

NOTE:

IT SHOULD BE NOTED THAT SOME ADJUSTMENTS ARE INTERDEPENDENT.

BRIGHTNESS AND CONTRAST SHOULD BE SET TO GIVE A NORMAL DISPLAY.

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CALIBRATION 2.5

1. **WORKSHOP TEST.** TEST "CHARGING SYSTEM"

   A. BATTERY VOLTS

   B. BATTERY RIPPLE

   C. AMPS

   D. RPM (CHECK)

2. **WORKSHOP TEST.** TEST "IGNITION SEC"

   A. PEAK KV.

   B. SPARK KV.

   C. SPARK DURATION (CHECK)

3. **MULTIMETER TEST.**

   A. KL1 VOLTS

   B. KL15 VOLTS

   C. STROBOSCOPIC TIMING

   D. VACUUM

   E. OIL TEMP.

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CALIBRATION :

1. A) BATTERY VOLTS **"CAL"**

B) **BATTERY RIPPLE "CAL"**

C) **AMPS "CAL"**

D) **RPM "CHECK"**

ALL CALIBRATION/CHECKS IN GROUP 1 ARE CARRIED OUT IN THE MULTIMETER TEST 1

MCS 2000 MODE :

VEHICLE ENTRY PAGE : 4 CYLINDERS
4 STROKE
NO MAG PROBE USED
PETROL
FIRING ORDER 1-3-4-2

SELECT MULTIMETER TEST 1

IS-100A **SETTINGS : - CYLINDERS TO 4**
- RPM TO 1000
- VOLT/OHMS TO 13 V
- RIPPLE OFF
- AMPS TO 80

CONNECTIONS :

- **RED CLIP BATTERY + TO THE** VOLT/OHM OUTPUT
- RED TRIGGER CLAMP TO THE TRIGGER LOOP
- SWITCH IS-100A ON

CHECK : - BATTERY VOLTS = 13 V
- ADJUST R **11 ON** THE SIGNAL INPUT **BD. IF NECESSARY**
- RPM = 1000
- ALT RIPPLE = 0 %
- AMPS = 0

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CONNECT THE DVM BETWEEN J 1 PIN 8 OF THE MUX A/D AND GROUND.

ADJUST R 40 ON THE AMP BOARD FOR 0.00 V.

PUT MCS 2000 THROUGH RECALIBRATION.

NOTE :

THE COMPUTER WILL ACCEPT AS ZERO ANY MUX VOLTAGE BETWEEN +/- 2.0 V. SHOULD THE VOLTAGE BE OUTSIDE THESE LIMITS THE TESTER WILL DISPLAY THE MESSAGE :

CALIBRATION

ADC REFERENCE	PASS
AMPS	FAIL
RIPPLE	PASS
ANALOG KV	PASS
VOLT/OHM	PASS
VACUUM	PASS
HC	PASS
CO	PASS
CO2	PASS

RETURN TO MULTIMETER TEST 1.

CONNECT THE GREEN CLAMP TO THE CURRENT COIL ON THE IS -100A SO THAT THE TESTER READS APPROXIMATELY :

- 80 AMPS

ADJUST R 1 ON THE AMP BOARD FOR -80 A +/- 1 AMP

(≈ +1.12 MUX VOLTS).

REVERSE POLARITY SWITCH.

CHECK TESTER READS + 80 A +/-3 AMPS(≈ +1.12 MUX VOLTS).

SWITCH IS-100A TO 200 AMPS,

CHECK TESTER READS 200 AMPS +/- 5 AMP(≈ +2.80 MUX VOLTS).

NOTE :

AMPS CALIBRATION MUST BE CHECKED WHEN THE AMP CLAMP IS CHANGED.

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WARNING:

THE AMP CLAMPS ARE FACTORY CALIBRATED AND SHOULD UNDER NO CIRCUMSTANCE BE ADJUSTED IN THE FIELD.

SWITCH IS-100A BATTERY RIPPLE ON.

CHECK :

ALT. RIPPLE = 11,5 % (=1.5 V PEAK TO PEAK RIPPLE SUPER-IMPOSED UPON A 13 V DC BATTERY LEVEL). ADJUST R 72 ON THE KV PROCESSOR BD. IF NECESSARY.
DISCONNECT MCS 2000 FROM IS-100A. SWITCH IS-100A OFF.

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2. A) PEAK KV "CAL"
B) SPARK KV "CAL"
C) SPARK DURATION "CHECK"

ALL CALIBRATION/CHECKS IN GROUP 2 ARE CARRIED OUT IN THE WORKSHOP TEST PROGRAM ON THE IGNITION SECONDARY TEST.

MCS 2000 MODE :

VEHICLE ENTRY PAGE : SAME AS IN GROUP 1.
WORKSHOP TEST.
IGNITION SECONDARY TEST PAGE 2.

IS-100A SETTINGS : - CYLINDERS TO 4
- RPM TO 1000
- RIPPLE OFF
- KV OFF
- SPARKLINE SLOPE OFF

CONNECTIONS :

- PATTERN LEAD TO PATTERN OUTPUT (REMOVE CHROME P.U.)
- RED TRIGGER CLAMP TO TRIGGER LOOP

SWITCH IS-100A POWER AND IGNITION ON.

CHECK:

KV-PEAK = 31.5 KV (ADJUST R 70 ON THE KV PROCESSOR BD. SLOT 4 ANALOG RACK IF NECESSARY).
KV-SPARK = 4.7 KV (ADJUST R 20 ON THE KV SLOPE BD. SLOT 2 ANALOG RACK IF NECESSARY).
MSEC = 2 MS (NOT ADJUSTABLE).

SWITCH SPARKLINE SLOPE TO ON.

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CHECK:

KV SPARK INCREASE TO 6 KV.

SWITCH : - SPARK LINE SLOPE OFF

KV ON

CHECK :

CYL. 3 PEAK KV = 13.7 KV.

DISCONNECT LEADS FROM IS-100

SWITCH IS-100A OFF.

3. a) KL 1 VOLTS
   b) KL 15 VOLTS
   c) STROBOSCOPIC TIMING
   d) VACUUM
   e) OIL TEMP.

   ALL CALIBRATION/CHECKS IN GROUP 3 ARE CARRIED OUT IN THE MULTIMETER TEST 1 AND 2.

   MCS 2000 MODE :

   VEHICLE ENTRY PAGE : SAME AS IN GROUP 1.

   MULTIMETER TEST 1.

   IS-100A SETTINGS : - CYLINDERS TO 4
   - RPM TO 1000
   - VOLTS/OHMS TO 13 V
   - RIPPLE TO OFF.

   CONNECTIONS:

   - KL 1 (GREEN CLIP) TO VOLT/OHM OUTPUT
   - KL 15 (YELLOW CLIP) TO VOLT/OHM OUTPUT
   - GROUND (BLACK CLIP) TO GROUND
   - RED CLAMP (TRIGGER) TO TRIGGER LOOP

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CHECK :

A) COIL -/KL 1 = 13 V
ADJUST R 14 ON THE INPUT BD. IF NECESSARY

B) COIL +/KL 15 = 13 V
ADJUST R 32 ON THE INPUT BD. IF NECESSARY

C) STROBOSCOPIC TIMING
SELECT MULTIMETER PAGE 2,

CHECK :

TIMING = 0° (ADVANCE KNOB ON REAR OF TIMING LIGHT IN THE ZERO DETENT POSITION).
ROTATE THE ADVANCE KNOB FULLY CLOCKWISE.

CHECK :

TIMING = 90°
ADJUST R 15 ON TIMING BD. IF NECESSARY

D) VACUUM

SELECT MULTIMETER TEST 2

STEP 1 : CONNECT THE DMM ON THE 20 V DC RANGE BETWEEN GROUND AND J1 PIN 12 OF THE MUX A/D (SLOT J 20 DIGITAL RACK).

STEP 2: CONNECT THE VACUUMTUBE TO A VACUUM SOURCE AND CALIBRATED VACUUM METER.

STEP 3: SWITCH ON TESTER.

STEP 4: ADJUST VACUUM SOURCE TO READ APPROXIMATELY 500 mB ON THE REF VACUUM METER.

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STEP 5: NOTE THE VOLTAGE READING ON THE DVM.

STEP 6: REMOVE VACUUM.

STEP 7: NOTE THE VOLTAGE READING ON THE DVM.

STEP 8: CALCULATE THE DESIRED VOLTAGE DIFFERENCE CORRESPONDING TO THE AMOUNT OF mB'S OF VACUUM APPLIED USING THE FOLLOWING CONVERSION.
1 mB = 4.5 mV
AFTER CALCULATION ENSURE RE-APPLIED VACUUM REMAINS CONSTANT AS SET IN STEP 4.

STEP 9: ADJUST R 4 ON THE MISCELLANEOUS FUNCTION BD. (SLOT 11 ANALOG RACK) FOR THE DESIRED VOLTAGE DIFFERENCE:
VOLTAGE DIFF. = VOLTS STEP 7 - VOLTS STEP 5.
EXAMPLE : 4.532 - 2.232 = 2.300 V DIFF.
FOR 500 mB V. DIFF = 500 X 415 mV = 2.25 V.
ADJUST 2.300 to 2.25 V

STEP 10: RE-APPLY THE VACUUM AND REPEAT STEPS 5, 6 AND 7 UNTILL THE DESIRED VOLTAGE DIFFERENCE IS ATTAINED:

STEP 11: REMOVE THE VACUUM AND ADJUST R 3 ON THE MISCELLANEOUS FUNCTION BD. TO READ 3.80 V.

STEP 12: PUT THE MCS 2000 THROUGH RECALIBRATION AND ENTER THE MULTIMETER PAGE 2.

STEP 13: RE-APPLY THE VACUUM AND BY SETTING VARIOUS VACUUM LEVELS BETWEEN 0 AND 500 mB CHECK FOR AN ACCURACY AND LINEARITY OF BETTER THAN +/- 5 mB OR 2 % BY COMPARING THE REF VACUUM METER TO THE VACUUM READING DISPLAYED ON THE MCS 2000.

STEP 14: REMOVE ALL EQUIPMENT.

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E) OIL TEMP.

PLACE TEMP PROBE IN BOILING WATER.

CHECK:

- OIL TEMP = 100°
  ADJUST R 2 ON THE INPUT BD. IF NECESSARY.

NOTE:

IF TEMP PROBE IS REPLACED RE-CALIBRATION WILL BE NECESSARY.

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SECTION 3

FUNCTIONAL DESCRIPTIONS

3.1 DIGITAL RACK

3.2 DISK DRIVE

3.3 VDU-ASSY

3.4 ANALOG RACK

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3.1

DIGITAL RACK

3.11 CENTRONICS INTERFACE BD.

3.12 FLOPPY DISC/RS232 INTERFACE BD.

3.13 ECPU68K BD.

3.14 RAM BD.

3.15 ECRT BD.

3.16 DIGITAL I/O BD.

3.17 KV CARDREADER BD.

3.18 MUX A/D BD.

3.19 PRE PROCESSOR BD.

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GENERAL

THE CENTRONICS INTERFACE BD. IS DESIGNED TO PROVIDE A STANDARD CENTRONICS OUTPUT THUS ALLOWING THE CONNECTION OF A PRINTER. IN ADDITION TO THIS FUNCTION THE BOARD ALSO ACTS AS A SWITCH BD. THAT ALLOWS THE VDU AND PRINTER TO BE SWITCHED BETWEEN THE HOST TESTER AND THE STL-2 OPTIONAL TEST LINK (FOR INFORMATION REGARDING THE TEST LINK SEE STL 2 SERVICE REPAIR MANUAL).

THE CENTRONICS INTERFACE BD. CAN BE SPLIT INTO TWO SEPERATE FUNCTIONS;PRINTER CONTROL/SWITCHING AND VIDEO SWITCHING.

VIDEO SWITCHING (REFER TO FIG. 1)

THE MCS MONITOR IS DESIGNED TO FUNCTION ON TTL VIDEO. IT IS THEREFORE NECESSARY TO SWITCH BOTH THE HORIZONTAL, VERTICAL SYNC SIGNALS AND THE VIDEO SIGNAL. THIS IS ACHIEVED USING A MULTIPLEXER AND RELAY.
A LED AT THE FRONT OF THE BOARD INDICATES THE VIDEO STATUS.

LED ON = STL VIDEO

LED OFF = HOST VIDEO

PREFERRED VIDEO SELECTION ON POWER-UP OR FORCED VIDEO SELECTION IS CONTROLLED BY PATCHING FIELD W3.

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PRINTER SWITCHING (REFER TO FIG.2)

THE PRINTER OPTION IN THE MCS 2000 IS DESIGNED TO OPERATE WITH BOTH THE HOST TESTER OR AN OPTIONAL STL 2 SYSTEM; THE SWITCHING OF THE PRINTER IS ACHIEVED USING A COMBINATION OF LATCHES AND MULTIPLEXERS. THE PREFERRED PRINTER CONNECTION ON POWER-UP OR FORCED PRINTER SELECTION IS CONTROLLED BY PATCHING FIELD W3. WITH THE BOARD PATCHED IN EITHER PREFERRED MODE THE CONTROL WILL BE HANDED TO SOFTWARE ON COMPLETION OF POWER-UP:

1. **PRINTER OUTPUT/INPUT UNDER CONTROL OF THE HOST TESTER:**

THE HOST TESTER CONTROLS THE PRINTER OUTPUT/INPUT VIA THE DIGITAL BACKPLANE. ADDRESS LINES Al THRU A 11 COMBINED WITH CONTROL LINES /LDSB, IO WAB AND IO RDB.THESE ARE BUFFERED AND THEN USED BY PAL (PROGRAMMABLE ARRAY LOGIC) U5 TO GENERATE THREE OUTPUTS, /CSl,/CS2 AND /CS3. THESE OUTPUTS ARE INTURN USED

A) **/CS1**

TO LATCH DATA ONTO THE DATA BUS TO THE PRINTER VIA U6.

/CS1 = /Al* / A2* / A3* / A4* /A5* / A6* / A7* / A8*/ A9* / Al0*/ All* /IOWR* / LDS

THIS FORMULA CORRESPONDS TO ADDRESS 800001 (OR 8XYOOl) WHERE X AND Y MAY BE O-F).

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B) /CS2

TO LATCH DATA INTO U7 WHICH IN TURN GENERATES STROBE AND HOST SELECT.
HOST SELECT IS USED TO OUTPUT ENABLE U6 AND SWITCH MULTIPLEXER U11 INTO THE HOST MODE;
STROBE IS MULTIPLEXED VIA U11 TO READ DATA INTO THE PRINTER.

/CS2 = A1* / A2* / A3* / A4* / A5* / A6* / A7* /A8* / A9* / A10* / A11* / IOWR* / LDS
THIS FORMULA CORRESPONDS TO ADDRESS 800003 (OR 8XY003 WHERE X AND Y MAY BE 0-F).

C) /CS3

TO SCAN SIGNALS FROM THE PRINTER VIA U3. SW SENSE IS ALSO SCANNED TO ENABLE THE HOST TESTER TO DETERMINE THE SWITCH STATUS OF THE BOARD.

/CS3 = A1* / A2* / A3* / A4* / A5* / A6* / A7* / A8* / A9* / A10* / A11* IORD
THIS FORMULA CORRESPONDS TO ADDRESS 800000 (OR 8XY000 WHERE X AND Y MAY BE 0-F).

AS MENTIONED IN THE INTRODUCTION SOME CONTROL LINES TO THE PRINTER ARE MULTIPLEXED BY U11.

THESE ARE :

STROBE - GENERATED AS EXPLAINED BY U7
PRIME - GENERATED BY THE CPU AS INITIAL
AUTO FEED - IN THE HOST MODE PATCHED BY W4

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2. PRINTER OUTPUT/INPUT UNDER CONTROL OF STL 2 SYSTEM.

THE PRINTER MAY BE USED AS AN OUTPUT DEVICE FOR AN STL 2 SYSTEM.
TO ACHIEVE THIS THE STL PULLS THE "STL SELECT" LINE LOW.
THIS CONNECTS ALL CENTRONICS SIGNALS FROM P3 THROUGH BUFFERS (U13, U12, U14) AND MULTIPLEXER (U11) TO THE PRINTER CONNECTOR P2. ALL CENTRONICS SIGNALS FROM THE MCS 2000 WILL BE DISABLED.

3. PATCHING (W1, W2, W3, W4, W6)

W3 SWITCHING CONTROL

AS PREVIOUSLY MENTIONED THE SWITCHING OF THE PRINTER AND VDU BETWEEN HOST AND STL AFTER POWER-UP IS UNDER SOFTWARE CONTROL. SWITCHING IS ACHIEVED BY :

1. THE HOST WRITING DATA TO U7 WHICH IN TURN CLOCKS U8.
OR
2. THE STL CLOCKING U8 DIRECTLY VIA ITS /STL SELECT LINE.

THE PATCHING OF W3 FIELD CAN EITHER BE USED TO FORCE A SWITCHING MODE THUS DISABLING THE SOFTWARE CONTROL, OR, IT MAY SELECT THE PREFERRED CONTROL SYSTEM ON POWER-UP.

THE SETTINGS ARE AS FOLLOWS :

MODE	W3
1 - FORCED TO MCS 2000	2-4 AND 5-6
2 - FORCED TO STL 2	5-7 AND 4-6
3 - PREFERENCE ON POWER-UP TO MCS 2000	3-4 AND 5-6
4 PREFERENCE ON POWER-UP STL 2	3-5 AND 4-6

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W1 + W2 OPTION PATCHING

THE HOST CPU IS ABLE TO DETERMINE WHAT OPTIONS ARE INSTALLED BY READING PATCHES W1 AND W2 VIA U3.

THE SETTINGS ARE AS FOLLOWS :

OPTION PRESENT	W1	W2	DB8	DB9
NONE	OUT	OUT	1	1
PRINTER	OUT	IN	1	0
STL 2	IN	OUT	0	1
STL 2 + PRINTER	IN	IN	0	0

W4 HOST AUTO FEED

THE HOST TESTER AUTO FEED SIGNAL FOR THE PRINTER IS PATCHED BY W4.

THE SETTING IS AS FOLLOWS :

AUTO FEED	W4
YES	OUT
NO	IN

W5 FRAME END

THE CENTRONICS BD. IS DESIGNED AS AN OPTION TO OPERATE WITH PRINTERS THAT REQUIRE A FRAME GROUND SIGNAL. IF SUCH A PRINTER IS USED W5 SHOULD BE PATCHED AS FOLLOWS :

	W5
PRINTER WITH FRAME GROUND	IN
PRINTER WITHOUT FRAME GROUND	OUT

NOTE:

FOR ALL PATCHING REQUIRED FOR THE SUN PRINTER SUPPLIED WITH THE OPTION KIT SEE SECTION 2.1 SET-UP.

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CENTRONICS INTERFACE BOARD

SIGNAL DESCRIPTION

CONNECTOR J1:

GROUND	0 VOLT LEVEL
+5v	+5V POWER
+12v	+12V POWER
DB0-DB15	DATA LINES D0-015 FROM DATA BUS
AB1-AB12	ADDRESS LINES A1-A12 FROM ADDRESS BUS
/INITIAL B	RESET SIGNAL FROM CPU BOARD
IORDB	I/O READ STROBE SIGNAL FROM CPU BOARD
IOWRB	I/O WRITE STROBE SIGNAL FROM CPU BOARD
/LDSB	LOWER DATA STROBE SIGNAL FROM CPU BOARD

CONNECTOR P2:

/STB	STROBE SIGNAL OUTPUT TO PRINTER
GROUND	0 VOLT LEVEL
DATA 0-7	DATA LINES 0-7 TO PRINTER
/ACK	ACKNOWLEDGE INPUT FROM PRINTER
BUSY	BUSY STATUS INPUT FROM PRINTER
PE	PAPER END INPUT FROM PRINTER
SELECT	PRINTER SELECT MODE SENSE INPUT
/PRIME	INITIALLIZATION OUTPUT TO PRINTER
/AUTO FEED	OUTPUT SIGNAL TO PRINTER FOR NEW LINE AFTER PRINTING
/ERROR	INPUT SIGNAL SENSES IF PRINTER IS IN ERROR STATUS
SIGNAL GROUND	0 VOLT LEVEL FOR SIGNAL LINES
FRAME GROUND	GROUND LEVEL FOR PRINTER CHASSIS

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CONNECTOR P3:

/STL STB	STROBE INPUT TO CONTROL PRINTER FROM STL 2
GROUND	0 VOLT LEVEL
STL DATA 0-7	DATA LINES 0-7 TO CONTROL PRINTER FROM STL 2
/STL ACK	ACKNOWLEDGE OUTPUT TO STL 2
STL BUSY	BUSY STATUS OUTPUT TO STL 2
STL PE	PAPER END OUTPUT TO STL 2
STL P SELECT	PRINTER SELECT OUTPUT TO STL 2
/STL PRIME	INITIALLIZATION INPUT FROM STL 2
/STL AUTO FEED	INPUT SIGNAL FROM STL 2 FOR NEW LINE AFTER PRINTING
/STL ERROR	OUTPUT SIGNAL TO STL 2 IF PRINTER IS IN ERROR STATUS
SIGNAL GROUND	0 VOLT LEVEL FOR SIGNAL LINES

CONNECTOR P4:

VIDEO IN	VIDEO INPUT FROM MCS 2000
HSIN	HORIZONTAL SINC INPUT FROM MCS 2000
VSIN	VERTICAL SINC INPUT FROM MCS 2000
GROUND	0 VOLT LEVEL FROM MCS 2000

CONNECTOR P5:

VIDEO STL	VIDEO INPUT FROM STL 2
STL HS	HORIZONTAL SINC INPUT FROM STL 2
STL VS	VERTICAL SINC INPUT FROM STL 2
/STL SELECT	SELECT LINE INPUT TO CONTROL THE “SWITCH” FROM STL
/STL SENSE	SENSE OUTPUT INDICATES STATUS OF THE "SWITCH" TO STL 2
GROUND **STL**	0 VOLT LEVEL

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CONNECTOR P6:

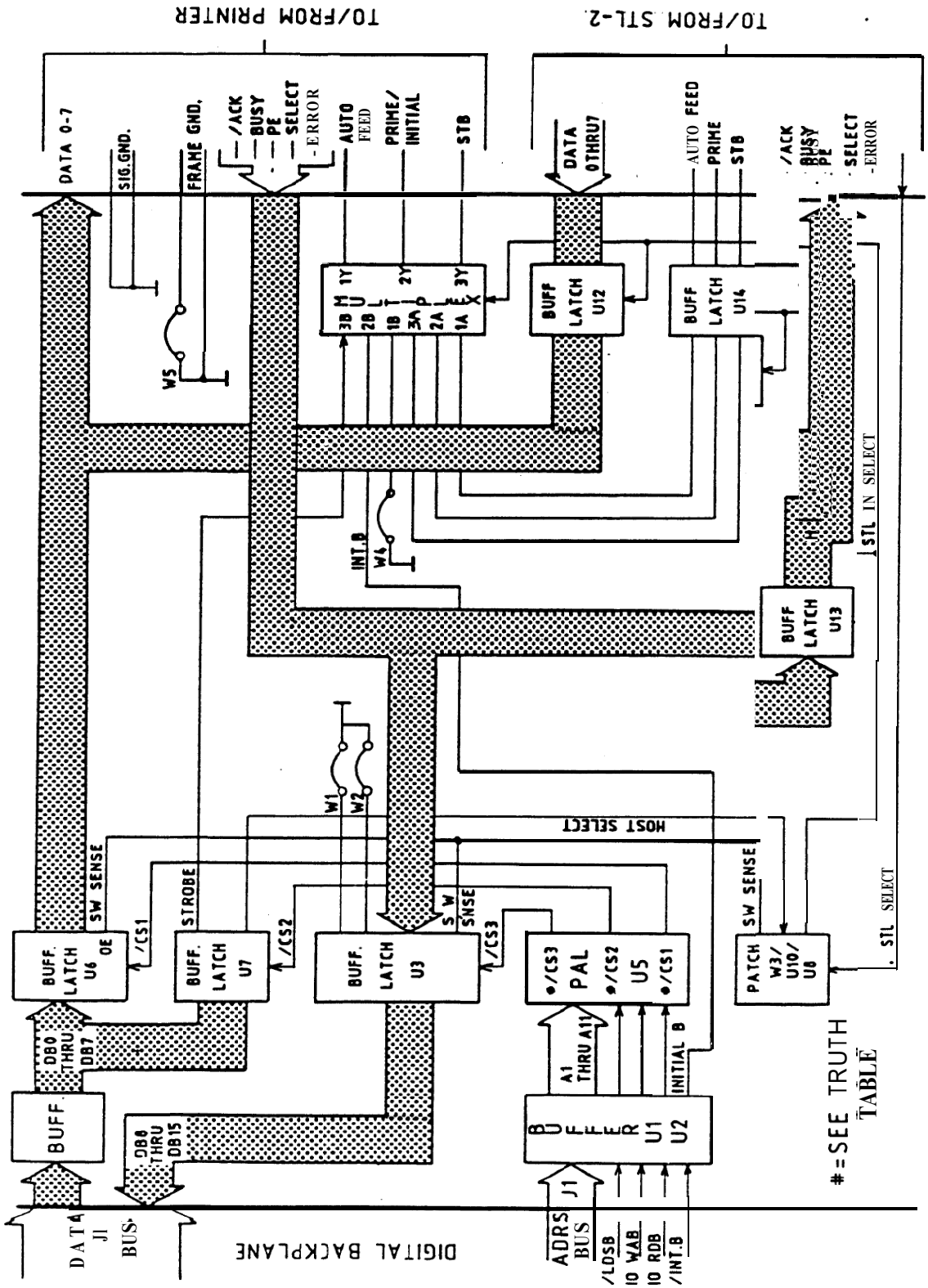
VIDEO OUT	VIDEO OUTPUT SIGNAL TO THE VDU
HS OUT	HORIZONTAL SINC SIGNAL TO THE VDU
VS OUT	VERTICAL SINC OUTPUT TO VDU
GROUND	0 VOLT LEVEL

GENERAL SIGNALS:

D0-D7	BUFFERED DATA LINES DB0-DB7
A1-A12	BUFFERED ADDRESS LINES AB1-AB12 (A12 IS NOT USED)
/LDS	BUFFERED LOWER DATA STROBE SIGNAL
IOWR	BUFFERED I/O WRITE SIGNAL
IORD	BUFFERED I/O READ SIGNAL
/INITIAL	BUFFERED INITIAL SIGNAL
/CS1	CLOCK SIGNAL FOR LATCH U6
/CS2	CLOCK SIGNAL FOR LATCH U7
/CS3	ENABLE SIGNAL FOR U3
/SW SENSE	ENABLE SIGNAL FOR OUTPUT FROM U6 AND "SWITCH" SENSE SIGNAL FOR MCS 2000
ACKS	ACKNOWLEDGE SENSE SIGNAL (SET BY /ACK SIGNAL FROM PRINTER)
/STBM	DATA STROBE SIGNAL FOR PRINTER FROM MCS 2000
/ACKB	BUFFERED /ACK SIGNAL FROM PRINTER
/STL IN SELECT	STL SELECT SIGNAL TO ACTIVATE BUFFERS TO CONTROL THE PRINTER AND VDU

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FIG. 2 PRINTER SWITCHING



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THE FLOPPY DISC/RS232 INTERFACE BD. IS SITUATED IN SLOT 15 OF THE DIGITAL RACK AND IS CONNECTED TO THE SYSTEM AS SHOWN IN **FIG. 1** (PAGE 14).

THE BOARD HAS TWO FUNCTIONS WITHIN THE **TESTER** :

1. TO LOAD DATA FROM DISC INTO THE RAM MEMORY BD.

2. TO PROVIDE TWO RS232 CHANNELS FOR TESTING PURPOSES AND/OR OPTIONAL COMMUNICATION LINKS WITH GAS BENCH, PRINTER, STL, ETC.

1. FLOPPY DISC INTERFACE (REFER TO FIG. 2).

THE FLOPPY DISC INTERFACE IS BASED AROUND A WD 1772-02 FLOPPY DISC CONTROLLER IC (U8). THIS IC IN COMBINATION WITH LATCH U9 IS CAPABLE OF HANDLING ALL SIGNALS TO AND FROM UP TO FOUR DISC DRIVES.
BI-DIRECTIONAL TRI-STATE BUFFER U3 RECEIVES AND TRANSMITS DATA BETWEEN THE ON BOARD DATA BUS AND BACKPLANE BUS.
THE CPU CAN READ THE PATCHING STATUS OF W11 THRU W17 AND THE DATA REQUEST SIGNAL FROM U8 VIA U7.

U8, U9, U3, U7 ARE CONTROLLED BY DECODING ADDRESS LINES A1 THRU A10 AND. CONTROL LINES I/O RD AND I/O WR.

THIS DECODING IS ACHIEVED VIA THE CHIP SELECT LOGIC COMPROMISING OF U1, U11, U5, U6, U13 AND U10 PATCHES W1 THRU W6 DETERMINE THE ADDRESS SETTINGS FOR THE DECODING.

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WITH THE PATCHES SET AS SHOWN IN **FIG.2** THE FOLLOWING ADDRESSES COMBINED WITH I/O RD **and** I/O WR TO PERFORM THE FOLLOWING FUNCTIONS.

STARTING ADDRESS	I/O RD	I/O WR	FUNCTION
8000C1		X	WRITE LATCHES U9 FOR FDC SET-UP*
8000C9*	X		READ STATUS REGISTER U8
8000C9		X	WRITE COMMAND REGISTER U8
8000CB*	X		READ TRACK REGISTER U8
8000CB		X	WRITE TRACK REGISTER U8
8000CD*	X		READ SELECTOR REGISTER U8
8000CD		X	WRITE SELECTOR REGISTER U8
8000CF*	X		READ DATA REGISTER U8
8000CF		X	WRITE DATA REGISTER U8
8OOOC1*			READ PATCHES W11 W17 AND DRQ VIA U7

*BI-DIRECTIONAL TRI-STATE BUFFER U3 IS REVERSED EVERY TIME THE BOARD IS CORRECTLY ADDRESSED IN THE READ MODE.

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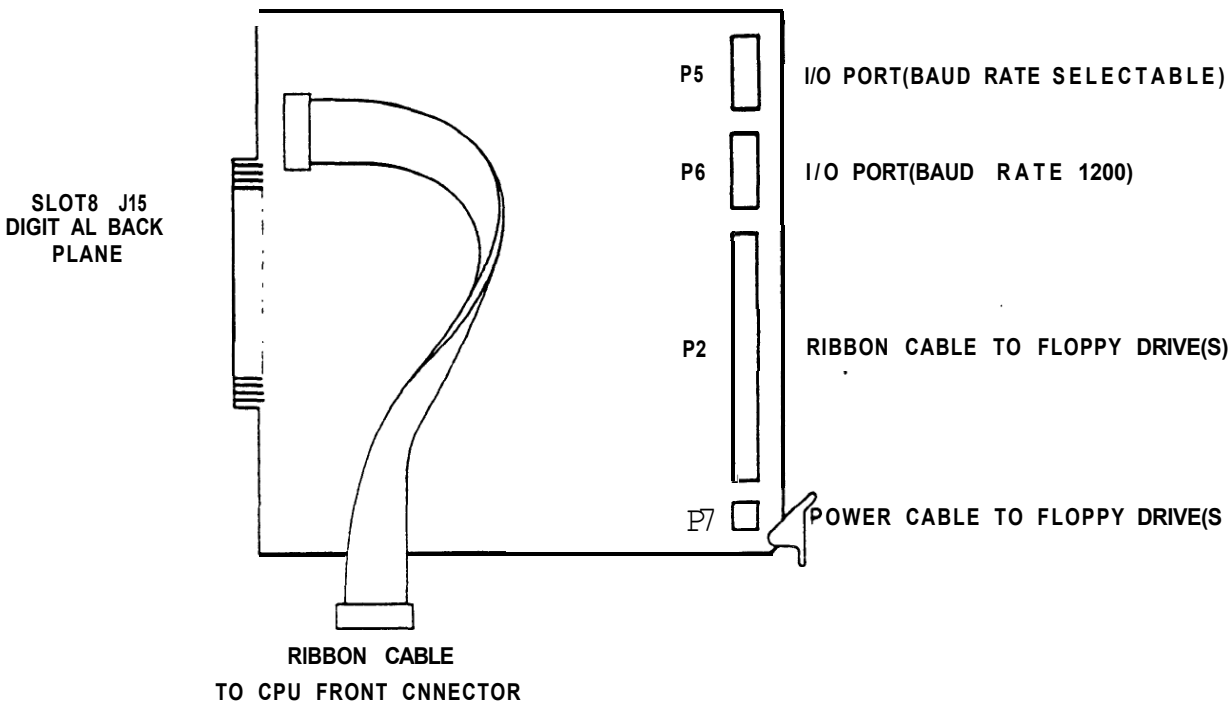
FLOPPY DISC CONTROLLER U8 REQUIRES SOME FURTHER CONTROL LINES.THESE ARE :

LINE	SOURCE	FUNCTION .
R/W	CPU BD.	SETS U8 IN ITS READ OR WRITE MODE
CLK	XTAL (U4, U10)	8MHz, CLOCK FOR FDC
/DDEN	U9	SET U 8 IN DOUBLE DENSITY MODE DURING INITIALISATION
/MR	U9*	RESETS U8 DURING INITIALISATION

U9* DERIVES RESET FROM INITIAL FROM DIGITAL BACKPLANE.

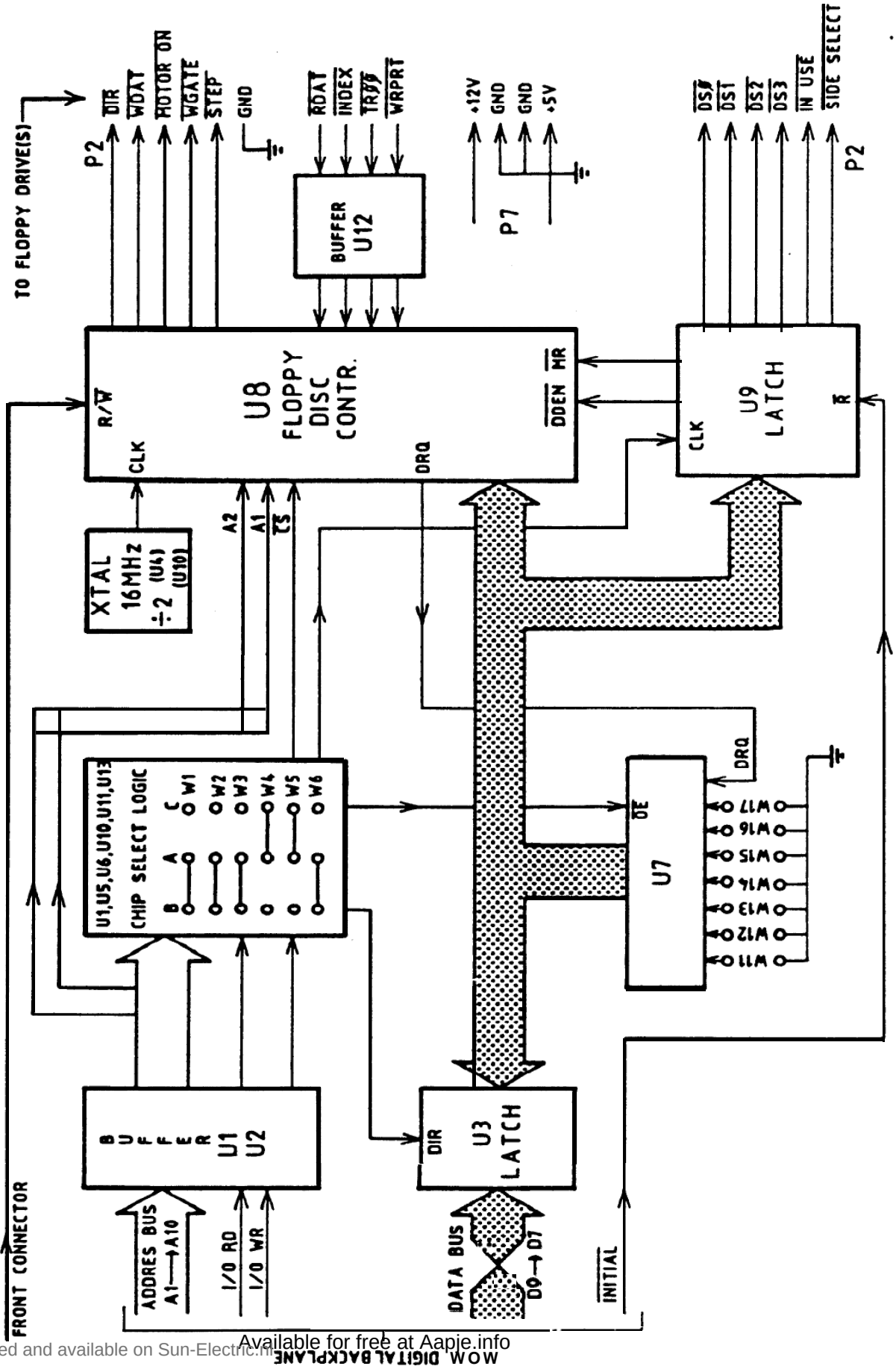
ADDRESS LINES 1 AND 2 SELECT DESIRED REGISTER IN U8.

FIG.1. GENERAL BLOCK DIAGRAM



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FIG 2 BLOCK DIAGRAM FLOPPY DISC CONTROL



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2: RS232 CHANNELS (REFER TO FIG 3)

AS EXPLAINED EARLIER THE FLOPPY DISC RS232 INTERFACE BOARD CONTAINS TWO RS232 COMPATIBLE OUTPUTS.

THESE TWO OUTPUTS ARE INDEPENDENT OF EACH OTHER AND BASED AROUND THEIR OWN 6551 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER. THESE DEVICES HANDLE ALL THE LINES TO AND FROM AN RS232 COMPATIBLE DEVICE.

ALL ADDRESS, CONTROL AND DATA LINES REQUIRED FOR THIS CIRCUIT ARRIVE FROM THE CPU, VIA THE FLAT RIBBON CABLE TO P4 (NOTE THE R/W SIGNAL IS ALSO USED BY THE FDC).

ADDRESS LINES A1 AND A2 ARE USED TO SELECT THE DESIRED REGISTER WITH THE COMMUNICATION INTERFACE.

ADDRESS LINES A3, A4, A5 IN COMBINATION WITH CONTROL LINE 6800 ARE ENCODED BY U18 AND U19 TO DERIVE THE CHIP SELECT LINES FOR THE TWO COMMUNICATION INTERFACES.

ON RECEIVING THE CHIP SELECT SIGNAL THE CORRESPONDING IC COMES OFF ITS TRI-STATE MODE AND DATA MAY BE WRITTEN TO OR READ FROM THE SELECTED REGISTER.

THE FOLLOWING ADDRESSES COMBINED WITH THE R/W LINE ENABLE THE FOLLOWING FUNCTIONS.

	ADDRESS	READ	WRITE	FUNCTION
	C000D1	X		READ DATA REGISTER
	C000D1		X	WRITE DATA REGISTER
CHIP	C000D3	X		READ STATUS REGISTER
SELECT	C000D3		X	RESET COMMAND REGISTER
U17	C000D5	X		READ COMMAND REGISTER
	C000D5		X	WRITE COMMAND REGISTER
	C000D7	X		READ CONTROL REGISTER
	C000D7		X	WRITE CONTROL REGISTER

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CONT.

	ADDRESS	READ	WRITE	FUNCTION
	COOOD9	X		READ DATA REGISTER
	COOOD9		X	WRITE DATA REGISTER
	COOODB	X		READ STATUS REGISTER
CHIP	COOODB		X	RESET COMMAND REGISTER
SELECT	COOODD	X		READ COMMAND REGISTER
U16	COOODD		X	WRITE COMMAND REGISTER
	COOODF	X		READ CONTROL REGISTER
	COOODF		X	WRITE CONTROL REGISTER

THE REMAINING SIGNALS FROM THE CPU PERFORM THE FOLLOWING FUNCTION WITHIN THE COMMUNICATIONS INTERFACE :

E = ENABLE CLOCK SIGNAL FROM CPU : TRIGGERS ALL DATA TRANSFERS BETWEEN THE CPU AND COMMUNICATIONS INTERFACE:

VMA/CS = 2ND CHIP SELECT LINE : MUST BE LOW TO SELECT CHIP GENERATED BY CPU AS VMA (VALID MEMORY ADDRESS) AFFECTS ADDRESS DECODING.

RES = CHIP RESET DURING INITIALLISATION

IRQ = INTERRUPT REQUEST SENT TO CPU : MAY BE USED FOR SOME RS232 APPLICATIONS E.G. SGA 9000 OPTION.

BAUDRATES

THE COMMUNICATIONS INTERFACE'S BAUDRATE IS PROGRAMMED DURING THE INITIALLISATION. THE PRESENT SOFTWARE PROGRAMS THE CHANNELS AS FOLLOWS :

P5 CHANNEL

THE BAUDRATE OF P5 CHANNEL IS PROGRAMMED ACCORDING TO THE SETTING OF PATCHES W11-W14.

DURING INITIALLISATION THE CPU FIRST READS THE STATUS OF THESE PATCHES VIA DATA LATCH U7 (SEE FDC INTERFACE) AND THEN PROGRAMS U16 ACCORDINGLY.

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BAUD RATE PATCHING TABLE (P5)

w14	w13	w12	W11	BAUDRATE
IN	IN	IN	OUT	50
IN	IN	OUT	IN	75
IN	IN	**OUT**	**OUT**	109,92
IN	OUT	IN	IN	134,58
IN	OUT	IN	**OUT**	150
IN	OUT	OUT	IN	300
IN	OUT	OUT	OUT	600
OUT	IN	IN	IN	1200
OUT	IN	IN	OUT	1800
OUT	IN	**OUT**	IN	2400
OUT	IN	**OUT**	**OUT**	3600
OUT	OUT	IN	IN	4800
OUT	**OUT**	IN	**OUT**	7200
OUT	**OUT**	**OUT**	IN	9600
OUT	**OUT**	**OUT**	**OUT**	19200

- **P6 CHANNEL**

  THE BAUDRATE OF P6 CHANNEL IS PROGRAMMED DURING INITIALLISATION AT A FIXED RATE OF 1200 BAUD.
  THE RS232 SIGNALS IN AND OUT OF U16 AND U17 CONFORM TO INDUSTRY STANDARDS AND ARE BUFFERED BY U21, U23 AND U22, U24 RESPECTIVELY.

PATCHES W9 AND W10

PATCHES W9 AND W10 ALLOW THE REVERSING OF PINS 8 AND 9, THE TXD AND RXD LINE OF BOTH CHANNELS. THIS INCREASES THE FLEXIBILITY OF CONNECTION TO OTHER SYSTEMS.

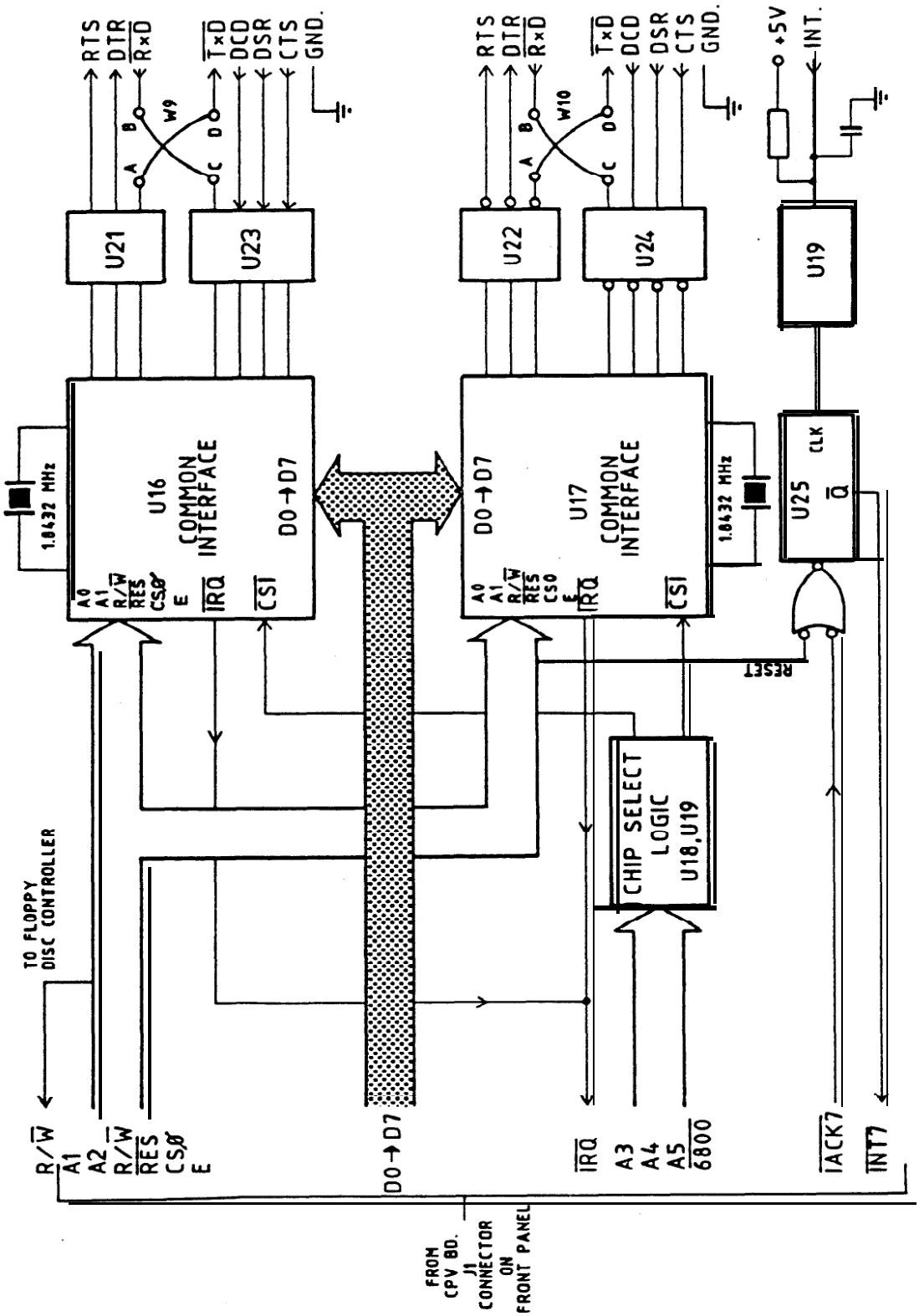
W17

W17 IS NOT USED WITH THE PRESENT SOFTWARE.

IMPORTANT

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FIG. 3 RS232 CHANNELS



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SIGNAL DESCRIPTION

+5v	+5VOLT POWER FROM J1 (BACKPLANE)
+5VL	+5VOLT POWER FROM P3, P4 (CPU)
+12V	+12VOLT POWER FROM J1 (BACKPLANE)
+12VL	+12VOLT POWER FROM P3, P4 (CPU)
-12VL	-12VOLT POWER FROM P3, P4 (CPU)
GND	0 VOLT LINE FROM J1 (BACKPLANE)
GNDL	0 VOLT LINE FROM P3, P4 (CPU)
A1-A10	ADDRESS LINES FROM ADDRESS BUS
BDO-BD7	BUFFERED DATA LINES
CTS	CLEAR TO SEND INPUT (RS232)
/CS1	CHIP SELECT LINE FOR U16, U17
CLK	CLOCK CYCLE FOR U8
/CS	CHIP SELECT LINE FOR U8
DO-D7	DATA LINES FROM DATA BUS
DCD	DATA CARRIER DETECT INPUT SIGNAL (RS232)
DSR	DATA SET READY INPUT SIGNAL (RS232)
DTR	DATA TERMINAL READY OUTPUT SIGNAL -12V or +12V (RS232)
DRQ	DATA REQUEST OUTPUT SIGNAL FROM U8

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/DDEN	DOUBLE DENSITY ENABLE INPUT SIGNAL TO U8
/DIR	DIRECTION CONTROL SIGNAL TO FLOPPY DRIVE
/DS0-/DS3	DRIVE SELECT SIGNAL TO FLOPPY DRIVE(S) (MAX 4 DRIVES)
E	ENABLE CLOCK SIGNAL TO CONTROL U16, U17
/IRQ	INTERRUPT REQUEST OUTPUT SIGNAL FROM U16, U17
/INT 7	INTERRUPT LEVEL 7 HIGHEST INTERRUPT LEVEL TO CPU
/IACK 7	INTERRUPT ACKNOWLEDGE ON LEVEL 7 FROM CPU
INT	INTERRUPT INPUT TO GENERATE /INT 7 ACTIVE FROM LOW TO HIGH
I/O WR	WRITE STROBE PULSE FROM CPU. ACTIVE ABOVE ADDRESS 7FFFFF
I/O RD	READ STROBE SIGNAL FROM CPU. ACTIVE ABOVE ADDRESS 7FFFFF
/INITIAL	RESET SIGNAL FROM CPU
/INDEX	INDEX PULSE INPUT FROM THE FLOPPY DRIVE
/IN USE	CONTROL SIGNAL TO FLOPPY DRIVE
/MOTOR ON	MOTOR ON SIGNAL TO FLOPPY DRIVE
/MR	MASTER RESET SIGNAL, RESETS U8
/RES	RESET SIGNAL FROM CPU
R/W	READ, WRITE LINE FROM CPU (HIGH DURING A READ CYCLE, LOW DURING A WRITE CYCLE)
RTS	REQUEST TO SEND OUTPUT FROM RS232 P5, P6
/RXD	RECEIVE DATA INPUT FROM RS232 P5, P6
RXC	RECEIVE CLOCK. TEST POINT FOR CLOCK PULSE FROM INTERNAL BAUDRATE GENERATOR (U16, U17)
/SSEL	SIDE SELECT CONTROL SIGNAL TO THE FLOPPY DRIVE (SELECTS SIDE OF FLOPPY DISC)
/RDAT	READ DATA LINE INPUT FROM THE FLOPPY DRIVE

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/STEP	STEP CONTROL OUTPUT FOR THE FLOPPY DRIVE'S HEAD
/TXD	TRANSMIT DATA OUTPUT FROM RS232 ON P5, P6
/TRØØ	TRACK 0 INDICATION INPUT SIGNAL FROM THE FLOPPY DRIVE
VMA	VALID MEMORY ADDRESS INPUT FROM CPU, INDICATE WHEN VALID MEMORY ADDRESS IS AVAILABLE
/W DAT	WRITE DATA OUTPUT LINE TO FLOPPY DRIVE
/ W GATE	WRITE GATE. WRITE CONTROL OUTPUT TO FLOPPY DRIVE
/WPRT	WRITE PROTECT INPUT LINE FROM FLOPPY DRIVE
/6800	6800 DEVICES SELECTION ACTIVE FROM ADDRESS C00000

3.1.3

0692E9305-90

FUNCTIONAL DESCRIPTION OF ECPU68K BOARD (assy 7001E9311-44) (schematic 7092E9311-47)

ORIGINATOR : G KOK
APPROVED : B Ge
DATE : 11-88
ERN : 0205
ECN :
REF. NR. : A3004

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INTRODUCTION

This document describes the function of the ECPU68K board.

Refer to : assy 7001E9311-44
schematic 7092E9311-47

The ECPU68K board replaces the older CPU/RAM board (7001E9004).
The ECPU68K board can be used in MCS2000, SUN2014 and SAM4000 testers.
Reasons for using the ECPU68K board are:
Increase of system reliability
Required for DIGITAL SCOPE option.

The ECPU68K board is deeigned to work in combination with the RAM board. It is not possible to combine an ECPU68K board with an older MEMORY board (7001E9311-12). This is due to the fact that the older MEMORY board (REV. C and up) wants to see a W/R signal on pin 47 of the bus connector, while the ECPU68K generates a R/W signal (inverted W/R) at pin 47 of the bus.

GENERAL

The ECPU68K board controls all digital boards in the tester-
Also the floppy disc drive, printer and most analog boards are controlled by the ECPU68K board.
The central part of the ECPU68K board is the 68000 micro processor. This is a 16 bit processor which can address 16 Mbyte of memory.
The processor controls the 'tester' via DATA BUS, ADDRESS BUS and CONTROL BUS.

The ECPU68K board fetches its Instructions and programmed limits from EPROM's and RAM's,
The EPROM's are located on the ECPU68K board itself.
The RAM's are located on the RAM board.
The ECPU68K board also uses RAM's for storage of temporary data or calibration constants, for intermediate calculations.

The ECPU68K board also contains an EEPROM (electrically erasable programmable read only memory). The size of the EEPROM is 2K*8.
The EEPROM is available to the processor for storage of information which the 'tester wishes to remember' after it has been powered down. As this chip is electrically erasable it is possible to alter the data it contains for such uses as customer programmed limits.

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FUNCTIONAL DESCRIPTION

ADDRESS BUFFERS

E5. F5 and D5 are address buffers. Addresses are generated by the 68000 processor. The buffers are used unidirectionally and are enabled continuously. CS buffers several control signals.
G2 is also an address or control signal buffer (unidirectional).

DATA BUFFERS

H5 and G5 are data buffers. Direction of data can be :
From 68000 processor to other device ; write operation.
From other device to 68000 processor ; read operation.

Direction of data is controlled by R/W signal (generated by 68000). Data buffers are enabled by /(/ONBOARD*AS), This means that the address strobe must be active (address is set) and the /ONBOARD signal must be false, i.e. data must go/come to/from other board than the ECPU68K board itself. /ONBOARD is active when reading or writing from/to EEPROM, EPROM or 68** family and during interrupt handling.
When output buffers are not selected the outputs remain in high impedance.

H2 is also a data buffer. It buffers data from/to floppy drive/ RS232 interface board. Only lower data bytes are used here. W/R signal controls direction of data. The buffer is enabled by /CSACIA. This signal is active when reading or writing from/to address C***D* or D***D* (* is don't care). (about 2Mbyte)

CLOCK OSCILLATOR

The clock signal is generated by a 8MHz crystal oscillator (X1). Flipflop G3 divides by two, so the 68000 processor runs at 4MHz. The 68000 processor divides the 4MHz clock by ten and feeds a 400KHz signal to pin 20 (E). This (E) signal is used as a clock frequency for the timers and ACIA's.

RESET CIRCUITRY

TL7705 (B1) takes care OF power-up reset (cold reset) and also takes care of a warm reset (reset button S1). During power-up B1 tests the supply voltage and keeps pin 5 low as long as the supply voltage has not reached its nominal voltage value. Making pin 2 low has the same effect. To ensure that the microprocessor system has reset, the TL7705 then initiates an internal time delay that delays the return of the reset output to the inactive state. The time delay is determined by capacitor C4.
In addition, when the supply voltage drops below the nominal value, the output will be active until the supply voltage returns to the nominal value. Capacitor C3 is connected to reduce the influence of fast transients in the supply voltage.

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EPROM's E3 and E4

The ECPU68K board contains two EPROM's. These EPROM's contain the boot software, operating system, initialisation instructions etc. (In case of an older tester configuration, these EPROM's were located on MEMORY board).
Four different types of EPROM's are possible :

2764 (8K*8)	jumpers	: W5 = 2-3 and W6 = 1-2
27128 (16K*8)	,,	: W5 = 2-3 and W6 = 1-2
27256 (32K*8)	,,	: W5 = 1-2 and W6 = 1-2
27512 (64K*8)		: W5 = 1-2 and W6 = 2-3

Standard the 27256 will be used.

The EPROM's are selected with /CSBOOT signal. The output is enabled by /LBRD (for EPROM E3 containing the low data bytes) and /HBRD (for EPROM E4 containing the upper data bytes).
/CSBOOT is active when reading in address range OOOOOO-OOFFFFhex.
/HBRD and /LBRD are derived from R/W,. W/R, /UDS and /LDS signals.
/LBRD is active when processor wants to read a lower data byte.
/HBRD is active when processor wants to read an upper data byte.
(lower data byte is DO-D7; upper data byte is D8-D15).

EEPROM F3 (F4) cq. RAM (F3,F4)

F3 is an electrically erasable programmable read only memory. The EEPROM is fully selfsupporting. After /CE signal (chip enable) goes active and a write command (/WR) is received the chip clears the allocated address and writes the new data byte to it. The programming voltage is internally generated. When busy the chip keeps /E2BUSY signal low. Programming one byte takes about 10 ms. The /E2BUSY signal must be high before the next byte can be written. In fact the /E2BUSY signal is not required. The program can introduce a fixed delay between two write actions- The time delay must be enough to allow the EEPROM to program a byte. Newer EEPROM's (e.g. 2864) do not have an /E2BUSY output.-The appropriate pin (1) is used for an extra address line (A15).

Location F4 can also contain an EEPROM (2864 only). This is for future use only.
Both locations F3 and F4 can contain RAM (32K*8). This is also for future use only.
Jumper W7 is out for 2817A only. When jumper W7 is in (for 2864 EEPROM or 43256 RAM), jumper W3 must be 1-2 (in case of DIGI-SCOPE) or out.
Jumper W3 may be In 2-3 position for I2817A only (not required since software uses a fixed delay between two write operations).

/CSE2 (chip select for F3 and F4) is active within address range 400000-4OFFFF- (64K range).
/HBRD and /LBRD; see EPROM paragraph.
/HBWR and /LBWR are derived from W/R, R/W, /UDS and /LDS.
/HBWR is active when processor wants to write an upper, byte.
/LBWR is active when processor wants to write a lower byte.
DO-D7 is lower byte.
D8-D15 is upper byte.

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TIMERS MC6840 (G4,H4)

G4 and H4 are programmable timer modules (PTM's). Each PTM contains three 16-bit binary counters which are under software control. The counters are used to cause system interrupts_ The PTM may be used for such tasks as frequency measurements, event counting, interval measuring and simular tasks.
By writing data bytes to the internal registers of the PTM's the mode of operation can be selected. When one of the internal timers has reached its programmed condition the PTM will interrupt the 68000 processor via the /IRQ1 (/IRQ2) line. (interrupt request). The 68000 processor reacts by making the chip select line of the appropriate PTH active (/CSTIM1,/CSTIM2) and reading the internal data registers of the PTM.

Inputs to the PTM's are a clock and gate for each individual counter. Inputs are tied to /INT2 thru /INT6,

H4 counter 1 : interrupts processor on 'end of ADC conversion'
H4 ,, 2 : ,, ,, ,, 'ENGINE SYNC pulses'
H4 ,, 3 : ,, ,, ,, 'CYLINDER CLOCK ,,'
G4 ,, 1 : ,, ,, ,, 'PREPROCESSOR READY'
G4 ,, 2 : used by software for several purposes
G4 ,, 3 : used as real time clock; interrupts every 100 ms.

PTM H4 is selected when /CSTIM2 is low and VMA (valid memory address) is high.
/CSTIM2 is low in address range C***B*hex and D***B*hex.
PTM G4 is selected when /CSTIM1 is low **and** VMA is high.
/CSTIM1 is low In address range C***E*hex and D***E*hex.
VMA is generated by the processor when reading or writing to address range COOOOO-DFFFFF. (2 Mbyte address space).
The E signal (400KHz) is the clock signal for the PTM's.

The RSO, RS1, RS2 inputs assign the internal register to/from which must be written/read. The R/W signal indicates either a read or write operation to the internal registers.
Data inputs/outputs are only active when both chip select inputs are in the truth state (/CSO = 0 and CS1 = 1).

LATCH I3 74LS273

The data latch 13 is used for :

a to enable or disable the 'TRIGGER SCOPE' flipflop.
b to latch data for the 'diagnostic LED's'.

The (trigger scope) flipflop B5 can generate /IRQ3 (interrupt request level 3).
Depending on jumper W3 setting the flipflop can be triggered by:

trigger signal derived from DIGITAL SCOPE BOARD.
or /E2BUSY signal from I2817A EEPROM.

A logic 0 on the 'D' input enables the flipflop to generate an /IRQ3 signal when clock input (11) goes high.
When jumper .W8 is out the flipflop is disabled continuously.
When set, the software can reset the flipflop by clearing it by making the /IACK3 signal (interrupt 3 acknowledge) low.

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The (preprocessor reset) flipflop B5 can generate the /PPRESET signal. This signal is used on the preprocessor board.
The state of the D-input (2) is clocked to the output (Q and /Q) when /CSREG (3) goes high. /CSREG can be generated by software. When set, the flipflop can be cleared by changing the state of the D-input (Dl> and generating a second /CSREG signal.

The clock signal /CSREG also clocks data (D2-D7) into latch I3.

The LED's can be used for diagnostic purposes. The software can control the LED's by writing a data byte to the latch 13.
For example; writing OOhex to latch I3 will illuminate all LED's, writing AFhex to latch 13 will illuminate LED's 2 and 4 (D6,D4 are logic 0).

/CSREG is generated when software reads or writes from/to address C***7* or D***7* (hexadecimal) (* = don't care).

DECODER PAL's A4 and B4

The decoder PAL's provide most control signals.
The control signals are derived from address lines and other 68000 processor signals. (See 7092E9311-47 sheet 6 for formulas).

STARTUP FLIPFLOP G3

Flipflop G3 (sheet 3 grid B3) is preset by /BRESET signal. This signal is active during power-up sequence or when Sl is pressed. When preset, the output signal STARTUP is high.
The flipflop is reset by the first write action (R/W = low)
The STARTUP signal is for future use only. (not used yet)

INTERRUPT PRIORITY ENCODER (B3)

B3 is a 8 to 3 line interrupt priority encoder. Inputs are numbered from 0 to 7. When one of the inputs is logic low, the output binary code is a function of the input number. When more inputs are active at the same time, only the highest numbered input is handled. The inputs are the interrupt request lines from several peripheral devices such as PTM's, EEPROM/TRSCOPE, RS232 etc. (n.b. the O-input is not used).

input of 74LS148	INTERRUPT INPUT(68000)			INTERRUPT LEVEL
1 2 3 4 5 6 7	/IPL2	/IPLl	/IPLO	
* * * * * * 0	0	0	0	LEVEL 7
* * * * * O 1	0	0	1	LEVEL 6
* * * * 0 1 1	0	1	0	LEVEL 5
* * * 0 1 1 1	0	1	1	LEVEL 4
* * O 1 1 1 1	1	0	0	LEVEL 3
* 0 1 1 1 1 1	1	0	1	LEVEL 2
0 1 1 1 1 1 1	1	1	0	LEVEL 1

(* = don'_t care)

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An interrupt on LEVEL 7 has the highest priority. An interrupt on this level is always accepted by the 68000 processor. This is called a non-maskable interrupt. The interrupts on a lower level are maskable. Which interrupts are masked depend on the interrupt-mask bits in the status register of the 68000 processor. When an interrupt is handled and a second (lower level) interrupt comes, the second interrupt is postponed. If the second interrupt has a higher level than the first interrupt, the second interrupt will be handled first.

SIGNAL LISTING

Refer to schematic 7092E9311-47 sheet 1 and 2 for signal listing and "where used" list.

SIGNAL DESCRIPTION

A1.... A23 (68000) Address bus. This 23 bit unidirectional three-state bus is capable of addressing 8 mega-words of data. It provides the address for bus-operation during all cycles except interrupt cycles.

BA1-..BA21 Buffered address bus.

AS, /AS Address strobe (resp. high **and** low active). Indicates that there is **a** valid address on the address bus.

DO.... D15 (68000) Data bus. This 16 bit, bidirectional, three-state bus is the general data path. It can transfer and accept data in either word or byte length.

BDO...BD15 Buffered data bus.

/LDS, /UDS Lower and upper data strobe. These signals control the data on the data bus as shown *in the* table below. When the R/W line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

/UDS	/LDS	R/W	D8.....D15	DO.....D7
high	high	----	no valid data	no valid data
low	low	high	8-15 valid	O-7 valid
high	low	high	no valid data	O-7 valid
low	high	high	8-15 valid	no valid data
low	low	low	8-15 valid	O-7 valid
high	low	low	O-7 valid **	O-7 valid
low	high	low	8-15 valid	8-15 valid **

** These conditions are a result of current implementation *in* 68000 processor and may not appear in future devices.

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/ BLDS, /BUDS Buffered lower and upper data strobe..

R/W Read/Write signal. This signal defines the data bus transfer as a read or write cycle. The R/W- signal also works in conjunction with the data strobes as explained above.

BR/W Buffered Read/Write signal.

W/R Write/Read signal (inverted R/W).

/DTACK Data transfer acknowledge. This input signal indicates that the data transfer is completed. When the processor recognizes /DTACK during a read cycle, data is latched and the bus cycle is terminated. When /DTACK is recognized during a write cycle, the bus cycle is terminated.

CLK, /CLK CLOCK. The (68000) clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor.

CLK4M Buffered CLK signal.

FCO, FCl, FC2 These FUNCTION CODE outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown below. The Information indicated by the function code outputs is valid whenever address strobe (/AS) is active.

FUNCTION CODE OUTPUT			CYCLE TYPE
FC2	FC1	FCO	
LOW	LOW	LOW	(undefined, reserved)
LOW	LOW	HIGH	user data
LOW	HIGH	LOW	user program
LOW	HIGH	HIGH	(undefined, reserved)
HIGH	LOW	LOW	(undefined, reserved)
HIGH	LOW	HIGH	supervisor data
HIGH	HIGH	LOW	supervisor program
HIGH	HIGH	HIGH	interrupt acknowledge

E ENABLE. This signal is the standard enable signal common to all 6800 peripheral devices. The period for this output is ten 68000 clock periods. (six clocks low, four clocks high). E is a free running clock and runs regardless of the state of the bus on the MPU.

/VMA, VMA VALID MEMORY ADDRESS. This output is used to indicate to 6800 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the peripheral is an 6800 family device.

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/VPA	VALID PERIPHERAL ADDRESS. This (68000) input indicates that the device or region addressed is a 6800 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use auto vectoring for an interrupt.
/BR	BUS REQUEST. This input can be wired ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master. This signal is not used on the ECPU68K-board!
/BG	BUS GRANT. This output indicates to all other potential bus master devices that the processor will release **bus** control at the end of the current bus cycle. This signal is not used on the ECPU68K-board!
/BGACK	BUS GRANT ACKNOWLEDGE. This input indicates that some other device has become the bus master. This signal is not used on the ECPU68K-board!
/BERR	BUS ERROR. This input informs the processor that there is a problem with the cycle currently being executed. This signal is not used on the ECPU68K-board!
/IPLO.../IPL2	These input pins indicate the encoded priority level of the device interrupt. Level seven is the highest priority while level zero Indicates that no interrupts are requested. See also text on page 6.
/IRQ1 /IRQ2 /IRQ3	INTERRUPT REQUEST. These lines are the input lines of the interrupt priority encoder (B3). From these lines the /IPLO, /IPL1 and /IPL2 are derived. See also text on page 6.
/IRQACIA	INTERRUPT REQUEST from ACIA on FLOPPY DISK-RS232 INTERFACE BOARD. Used when SGA9000 gasbench is connected. Input of interrupt priority encoder. See also text on page 6.
/INT2	INTERRUPT 2. This input to ECPU68K-board indicates an END OF A/D CONVERSION. Via PTM (H4) this can result in an INTERRUPT REQUEST to the 60000. (/IRQ2)
/INT3	INTERRUPT 3. This input to ECPU68K-board indicates an ENGINE SYNC occurrence. Via PTM (H4) this can result in an INTERRUPT REQUEST to the 68000.(/IRQ2)
/INT4, INT4	INTERRUPT 4. This input to the ECPU68K-board indicates a CYLINDER CLOCK occurrence. Via PTM (H4 this can result in an INTERRUPT REQUEST to the 68000. (/IRQ2)

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/INT5, INT5	INTERRUPT 5. This input to the ECPU68K-board can indicate a CYLINDER CLOCK occurrence. (Active when CYLINDER CLOCK signal is high) Future use only!
/INT6	INTERRUPT 6. This input to the ECPU68K-board indicates a PREPROCESSOR READY STATE. Via PTM (G4) this can result in an INTERRUPT REQUEST to the 68000 processor. (/IRQ1)
/IACK	INTERRUPT ACKNOWLEDGE. Indicates that an interrupt is recoqnized. Active when FC0, FC1 and FC2 are all high.
/IACK3	INTERRUPT ACKNOWLEDGE 3. Indicates that an interrupt from DIGITAL SCOPE BOARD or from I2817A-EEPROM (depending on jumper W3 setting) is recognized. Clears flipflop B5.
/IACK7	INTERRUPT ACKNOWLEDGE 7. Indicates that an interrupt from FLOPPY DISK-RS232 INTERFACE BOARD is recognized, Clears flipflop U25 on FLOPPY DISK-RS232 INTERFACE BOARD.
/CSACIA	CHIP SELECT ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER. This signal selects the DATA BUFFER H2. When active, data go/come to/from ACIA's on the FLOPPY DISK-RS232 INTERFACE board. Active in address range C***D* and D***D*. * = don't care.
/CSBOOT	CHIP SELECT BOOT. This signal selects both EPROM's E3 and E4. Active in address range OOOO-FFFF.
/CSE2	CHIP SELECT EEPROM. This signal selects locations F3 and F4. These locations can contain EEPROM *or* RAM. Active In address range 400000-40FFFF.
/CSTIM1	CHIP SELECT TIMER 1. This signal selects PTM G4. Active in address range C***E* and D***E*. * = don't care.
/CSTIM2	CHIP SELECT TIMER 2. This signal selects PTM H4. Active in address range C***B* and D***B*. * = don't care.
/CSREG	CHIP SELECT REGISTER. This signal selects register 13 and clocks the preprocessor-reset flipflop B5. Active in address range C***7* and D***7*. * = don't care.
/E2BUSY	EEPROM (I2817A only) BUSY **signal.** Active during the time that I2817A is internally writing a byte.
/HBRD	HIGH BYTE READ. Active when processor reads a high data byte. Derived from /UDS and R/W signals. See also /UDS on page 7.

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/LBRD	LOW BYTE READ. Active when processor reads a low data byte. Derived from /LDS and R/W signals. See also /LDS on page 7.
/HBWR	HIGH BYTE WRITE. Active when processor writes a high byte. Derived from /UDS and R/W signals. See also /UDS on page 7.
/LBWR	LOW BYTE WRITE. Active when processor writes a low byte. Derived from /LDS and R/W signals. See also /LDS on page 7,
/IORD, IORD	INPUT/OUTPUT READ. Active when data from input or output devices (e.g. FLOPPY INTERFACE) must be read- Active in address range 800000-BFFFFF,
/IOWR, IOWR	INPUT/OUTPUT WRITE. Active when data is written to input or output devices (e.g. FLOPPY INTERFACE). Active in address range 800000-BFFFFF.
/MEMEN	MEMORY ENABLE. Buffered /ADDRESS STROBE (/AS). See /AS on page 7.
/MEMRD	MEMORY READ. Active during reading from memory board, Active in address range OOOOOO-3FFFFF.
/MEMWR	MEMORY WRITE. Active during writing to memory board. Active in address range OOOOOO-3FFFFF.
/ONBOARD	ONBOARD. Active when data transfer is in following address ranges; OOOOOO-OOFFFF EPROMS on ECPU68K board. 400000-7FFFFF EEPROM plus not used space. C00000-FFFFFF 6800 family devices. The ONBOARD signal deselects data buffers HS and G5 when data transfer is between devices on the ECPU68K board itself.
STARTUP	STARTUP. This signal is only active after a power-up or reset cycle. It provides the possibility to relocate the memory map on the first write cycle (after the EPROM is read). When R/W signal goes low, the startup flipflop is reset. This feature is future use only !!
/PPRESET	PREPROCESSOR RESET. Generated by the preprocessor reset flipflop B5. B5 is under software control. This signal is used on PREPROCESSOR BOARD.
/RESET	RESET. This bidirectional signal acts to reset (start a system initialization sequence) the processor in response to an external reset signal (generated by TL7705). An internally (in 68000) generated reset (result of a /reset instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external

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devices is the result of external /HALT and /RESET signals applied at the same time.

/HALT — HALT. When this bidirectional line is driven by an external device (TL7705 in our case), it will cause the processor to stop at the completion of the current bus cycle. All control signals become inactive and all three-state lines are put in their high-impedance state.

/BRESET — BUFFERED RESET. Buffered output from TL7705 or 68000 /RESET line.

/INIT — INITIALIZE. Derived from /BRESET. Initializes peripherals on a power-on or reset cycle.

READY — READY. This signal comes from CRT-controller board When low it holds of the /DTACK signal to the processor. The processor then generates wait-cycles until READY signal goes high again. This feature allows the CRT controller or CRT RAM to read/write data from/to the 68000 processor when possible. Data transfer between CRT controller board and 68000 processor is only possible when CRT controller or CRT RAM are not occupied by a display cycle.

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3.1.4

0692E9305-91

FUNCTIONAL DESCRIPTION OF RAM-BOARD (assy 7001E9311-48) and ERAM-BOARD (assy 7001E9311-49)

ORIGINATOR : G KOK
APPROVED : B Ge
DATE : 11-88
ERN : 0285
ECN :
REF. NR. : A3005

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INTRODUCTION

This document describes the function of the RAM board and the ERAM board.

RAM board : assy 7001E9311-48 , schematic 7092E9311-51
ERAM board : assy 7001E9311-49 , schematic 7092E9311-52

These boards can be used in MCS2000 , SAM4000 and SUN2014 testers.

There is no big difference between these boards. Both boards make use of the same printed circuit (7025E9310-57).

The RAM board is designed to combine with an ECPU68K board. The ECPU68K board (assy 7001E9311-44) is the processor board of the system. This ECPU68K board is a replacement for the older CPU/RAM board (7001E9004). When a DIGITAL SCOPE option is to be installed, an ECPU68K board is required and, also a RAM board is required.
The RAM board replaces the older MEMORY board (7001E9311-12).

The ERAM board is designed to combine with the existing CPU/RAM board. The CPU/RAM board (7001E9004) must be at least revision D !!
The ERAM board also replaces the older MEMORY board (7001E9311-12).

The main difference between RAM board and ERAM board is that the ERAM board contains two EPROMS (boot-firmware) and the RAM board does not contain EPROMS (EPROMS are now located on ECPU68K board.

Reasons for replacing the older MEMORY board (7001E9311-12) by the RAM board or ERAM board are :
- Increase of memory size (required for DIGITAL SCOPE)
- Increase of system reliability.

Reasons for replacing the older CPU/RAM board (7001E9004) by the ECPU68K board are :
- Required for DIGITAL SCOPE option
- Increase of system reliability.

It must be noted that best system reliability requires both the ECPU68K board and the RAM board.

Due to the fact that the ERAM board contains EPROMS and the RAM board does not, there is also a difference in memory arrangement on both boards. Therefore the ROM C3 and jumper settings differ on both boards.

When necessary an ERAM board can be changed into a RAM board :
- Remove EPROMS (locations A1 and A2).
- Replace PROM C3 by 0703E0381-01.
- Set jumpers according schematic 7092E9311-51.

When necessary a RAM board can be changed into an ERAM board :
- Install EPROM firmware (2 EPROMS) in locations A1 and A2.
- Replace PROM C3 by 0703E0391-01.
- Set jumpers according schematic 7092E9311-52.

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MEMORY SIZE

The size of the older MEMORY board was 16 locations of 32K bytes each. This makes 512K bytes. This is including 2 EPROMS. (2*32K) So, 448K bytes of RAM memory.

The RAM board and the ERAM board contain 20 RAM chips of 32K bytes each. So each board contains 640K bytes of RAM memory.

Besides the 640K RAM memory the ERAM board contains also 64K of EPROM memory.

The increase of memory on the RAM board and ERAM board is required for the DIGITAL SCOPE option. Future software expansions may also require more memory size.

Both the RAM board and the ERAM board are prepared for extra memory expansions. (Future use only)
The RAM board can contain a maximum of 32 RAM chips of 32K each. This makes 1024K bytes of RAM memory to be the maximum.
There is no EPROM memory on the RAM board.

The ERAM board can contain a maximum of 28 RAM chips of 32K each. This makes 896K bytes of RAM memory to be the maximum.
There is also 64K of EPROM memory on the ERAM board.

MEMORY ARRANGEMENT ON RAM BOARD

RAM chips are selected by use of the CHIP SELECT signal. By making this signal active for 2 RAM chips (one for the lower DATA byte and one for the upper DATA byte) only, all RAM's outputs are in high impedance except the outputs of the selected RAM's,
The table below indicates in which memory range the appropriate RAM chips are selected: (addresses are in HEXADECIMAL notation)

00000 - 0FFFF	Reserved for EPROMS on ECPU68K board			
10000 - 1FFFF	RAM chips	H1 and H2	bottom	
20000 - 2FFFF	,,	H1 ,, H2	top	
30000 - 3FFFF	,,	G1 ,, G2	bottom	
40000 - 4FFFF	,,	G1 ,, G2	top	
50000 - 5FFFF	,,	F1 ,, F2	bottom	
60000 - 6FFFF	,,	F1 ,, F2	top	
70000 - 7FFFF	,,	E1 ,, E2	bottom	
80000 - 8FFFF	,,	E1 ,, E2	top	
90000 - 9FFFF	,,	D1 ,, D2	bottom	
A0000 - AFFFF	,,	D1 ,, D2	top	
B0000 - BFFFF	,,	C1 ,, C2	bottom	(expansion)
C0000- CFFFF	,,	B1 ,, B2	bottom	,, ,,
D0000 - DFFFF	,,	A1 ,, A2	bottom	,, ,,
E0000 - EFFFF	,,	C1 ,, C2	top	,, ,,
F0000 - FFFFF	,,	B1 ,, B2	top	,, ,, ,,
100000 - 10FFFF	,,	A1 ,, A2		,, ,,

A1.... H1 : lower data byte (D0-D7)
A2....H2 : upper data byte (D8-D15)

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MEMORY ARRANGEMENT ON ERAM BOARD

00000 - 0FFFF	EPROMS	A1 and A2	(bottom only)	
10000 - 1FFFF	RAM chips	H1 and H2	bottom	
20000 - 2FFFF	,,	H1 ,, H2	top	
30000 - 3FFFF	,,	G1 ,, G2	bottom	
40000 - 4FFFF	,,	G1 ,, G2	top	
50000 - 5FFFF	,,	F1 ,, F2	bottom	
60000 - 6FFFF	,,	F1 ,, F2	top	
70000 - 7FFFF	,,	E1 ,, E2	bottom	
80000 - 8FFFF	,,	E1 ,, E3	top	
90000 - 9FFFF	,,	D1 ,, D2	bottom	
A0000 - AFFFF	,,	D1 ,, D2	top	
B0000 - BFFFF	,,	C1 ,, C2	bottom	(expansion)
C0000 - CFFFF	,,	B1 ,, B2	bottom	,, ,,
D0000 - DFFFF	,,	C1 ,, C2	top	,, ,,
E0000 - EFFFF	,,	B1 ,, B2	top	,, ,,

A1....H1 : lower data byte (D0-D7)
A2....H2 : upper data byte (D8-D15)

RAM board and ERAM board: Address decoding is done by PROM's C3 and G3 and PAL C4. PAL DECODER C4 also generates several control signals.

ADDRESS BUFFERS

C5,D5 and D4 are address buffers. They also buffer upper and lower data strobe signals and the processor clock signal (4MHz). The buffers are unidirectional and are enabled continuously.

DATA BUFFERS

G5 and F5 are data buffers. Direction of data is controlled by /BUFDIR signal. The buffers are only enabled when required. Enable signal is /BUFEN. Both /BUFEN and /BUFDIR are generated by PAL DECODER C4.

BUFEN=DECEN=MEMRD*MEMEN*/A21+MEMWR*MEMEN"/A21
This implies that /BUFEN is active when reading or writing from/to address range : 000000 - 1FFFFF (2 Mbyte range)

BUFDIR=READ*W4+/READ*/W4
This implies that /BUFDIR depends on the R/W signal (bus 47) and the jumper W4 setting.
The older CPU/RAM board (REV D and up) generates a W/R signal on bus 47 and the newer ECPU68K board generates a R/W signal on bus 47 (inverted W/R). With jumper W4 the appropriate signal can be selected.
During a read operation data go from memory to processor board.
During a write operation data go from processor to memory board.

ECPU68K (7001E9311-44) board is used : jumper W4 must be installed.
CPU/RAM (7001E9004) board is used : Jumper W4 must be removed.

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DELAYED /HBRD AND /LBRD

Due to the fact that EPROMS consume very high current peaks when both CHIP SELECT signal and OUTPUT ENABLE signal go to the active state at the same *time, level* shifts in the ground (return) lines can occur. This can result in data errors; e.g. a transmitted '1' can be received as a '0'. (RAM's show this problem less)
When OUTPUT ENABLE signal is delayed from CHIP SELECT signal the problem will not occur.

PAL DECODER C4 generates the /DELDS3 signal. This is in fact a delayed 'memory read' signal. The delay is about 320 ns.
The delay is possible by 'gating' the MEMRD and MEMEN signals with the processor CLK4M signal (done in C4).
Generating /HBRD and /LBRD signals is done by 'gating' /DELDS3 signal with /UDS and /LDS signals. (upper/lower data strobe)
/HBRD and /LBRD are the OUTPUT ENABLE signals for RAM's and EPROM's,

JUMPER SETTINGS

If locations A1 and A2 contain EPROM's (256K) : W1 = 1-2
W2 = 1-2
W3 = 1-2

If locations A1 and A2 contain EPROM's (512K) : W1 = 1-3
W2 = 1-2
W3 = 1-2

If locations A1 and A2 contain RAM's (256K) : W1 = 1-4
W2 = 2-3
W3 = 2-3

If processor board is ECPU68K : W4 = IN.
If processor board is CPU/RAM (REV. D and up) : W4 = OUT.

PAL DECODER and PROM DECODER's

Refer to schematic 7092E9311-51 sheet 3 for RAM board DECODER PAL and DECODER PROM's information.
Refer to schematic 7092E9311-52 sheet 3 for ERAM board DECODER PAL and DECODER PROM's information.

SIGNAL LISTING

Refer to schematics 7092E9311-51 and 7092E9311-52 sheet 1 for signal listing.

SIGNAL DESCRIPTION

BA1 - BA21 Address lines from address bus (generated on CPU).

BD0 - BD15 Data lines from/to data bus.

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MEMRD	Memory read signal from CPU. Active only below 400000hex.
MEMWR	Memory write signal from CPU. Active only below 400000hex.
/MEMEN	Memory enable signal from CPU. In fact a buffered address strobe.
CLK4M	Clock signal from CPU. (4MHz))
BR/W	Read / write signal from CPU.
/BUDS	Upper data strobe from CPU. Active for D8 - D15.
/BLDS	Lower data strobe from CPU- Active for DO - D7.
A1 - A21	'on-board' address lines. Buffered BA1-BA21 signals.
DO - D15	'on-board' data lines. Buffered BDO - BD15 signals.
/UDS	Buffered /BUDS signal.
/LDS	Buffered /BLDS signal.
/DELDS3	Delayed 'mem read' signal.
/LBWR	Low byte write signal (Active below 200000hex). Active when writing DO-D7 to memory.
/HBWR	High byte write signal (Active below 200000hex). Active when writing D8-D15 to memory.
W4	+5V or GND depending on jumper W4.
/BUFDIR	Ruffered direction signal. Controls direction of data.
/BUFEN	Buffered enable signal (Active below 2OOOOOhex). Enables/disables data ports G5 and F5.
/DECEN	Decoder prom's enable signal (Active below 200000) Enables/disables DECODER PROM's G3 and C3.
/CS1B-/CS8B	Chip select signals for bottom RAM's (EPROM's)_
/CS1T-/CSBT	Chip select signals for top RAM's (EPROM's).
/HBRD	High byte read signal. (Active below 200000hex).
/LBRD	Low byte read signal. (Active below 200000hex).
R/W	Buffered BR/W signal .

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3.1.5

0692E9306-08

FUNCTIONAL DESCRIPTION OF ECRT-BOARD
P/N 7001E9311-59

ORIGINATOR : G.KOK / O.EERENBERG
CHECKED : P.TEL
APPROVED : B.GEE
DATE : FEBR. 1990
ERN : 0411
REF.NR. : A3012

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Preface:

This document describes the new ECRT-board (P/N 7001E9311-59), used in the MCS 2000.
The reasons for developing a new CRT-board are that components from the old CRT-controller board (P/N 7001e9311-14) such as:

- CRT-controller chip (CRT5037)
- RAM (2112)

are getting obsolete. Another reason for developing a new ECRT-board is the fact that additional character sets need to be available. (e.g./ Hebrew)

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Introduction:

The ECRT controller (6845) generates the signals necessary to interface a digital system to a raster scan CRT display. In this type of display, an electron beam starts in the upper left hand corner, moves quickly accross the screen and returns. This action is called a horizontal scan. After each horizontal scan the beam is incrementally moved down in the vertical direction until it has reached the bottom. At this point one frame has been displayed, as the beam has made many horizontal scans and one vertical scan. Two types of raster scanning are used in CRT's, interlace and non interlace. On the ECRT-board non-interlaced scanning is used. See fig. 1.

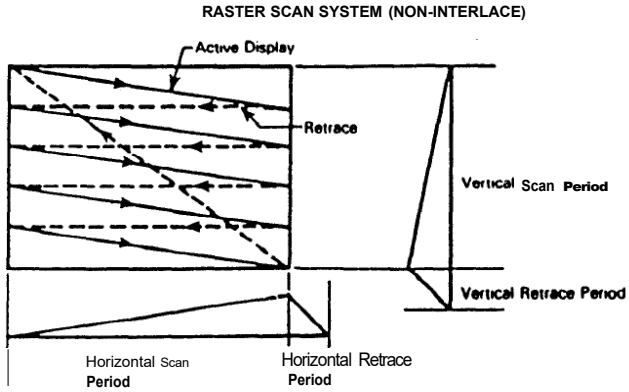


Figure 1.

Non-interlace scanning consists of one field per frame. The scan lines in figure 1. are shown as solid lines and the retrace patterns are indicated by the dotted lines. Increasing the number of frames per second will decrease the flicker. Ordinarily, either 50 or 60 frames per second refresh rate is used to minimize beating between the CRT and the power line frequency. This prevents the displayed data from weaving. In order to display the characters on the CRT screen the frames must be continually repeated. The data to be displayed is stored in the refresh (screen) memory by the ECPU68K controlling the data processing system. The data is usually written in ASCII code, so It cannot be directly displayed as characters. A character generator ROM is typically used to convert the ASCII code into the " dot " pattern for every character. The most common method of generating characters is to create a matrix of X*Y dots. As " x " and " Y " get larger a more detailed character may be created. Two common dot matrices ar 5 * 7 and 7 * 9. Many variations of these standards will allow Chinese, Japanese, or Arabic letters instead of English. Since characters require some space between them, a character block larger than the character is typically used. Available forms are shown in Figure 2.

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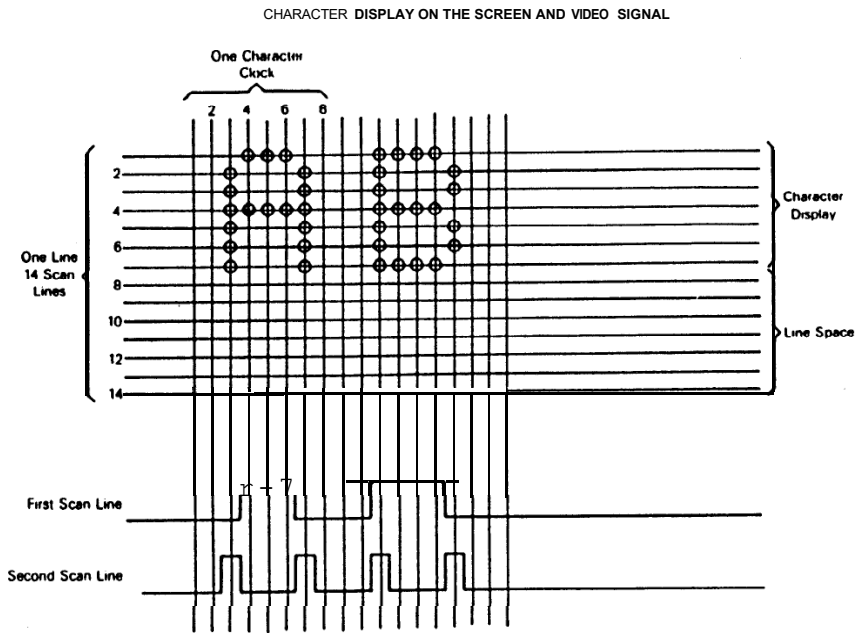


Figure 2.

The figure also shows the corresponding timing and levels for a video signal that would generate the characters. Because the ECRT-board has to produce the same screen format as the old one we use a matrix of 16 * 15 dots, where the characters are 9 dots high and 14 dots wide. There is a horizontal space between two characters (as we shall see later on, this space consists of 4 dots ; 2 dots from the matrix plus 2 fixed spaces).
The vertical space is 6 lines. There are 16 character rows and on each row we have 32 characters.

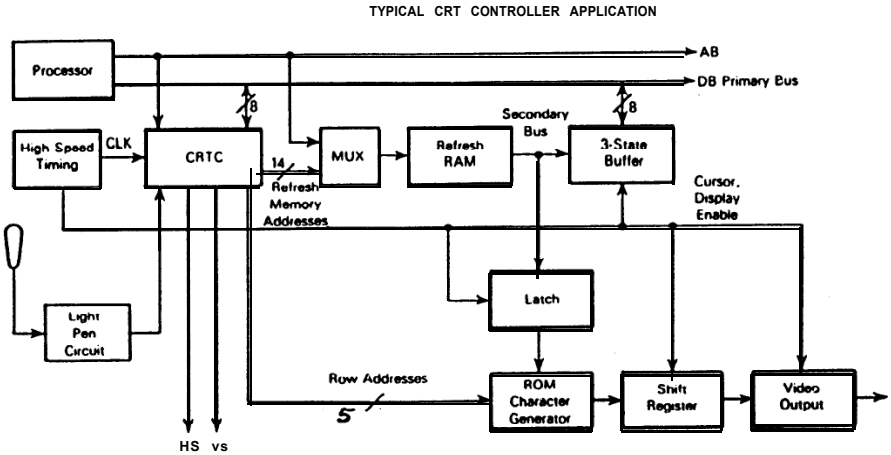


Figure 3.

Refering to figure 3.
The CRT controller generates the refresh addresses (MAO-MA13), row addresses (RAO-RA4) and the video timing (vertical sync,- VS-, horizontal sync, - HS -, and display enable, - DE -). Other

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functions include an internal cursor register which generates a cursor output when its contents correspond to the current refresh address. A light pen strobe input signal allows capture of the refresh address in an internal light pen register. All timing in the CRT controller is derived from the CLK input. In alphanumeric terminals, this clock signal is the character rate. The video rate or " dot " clock, is externally divided by high speed logic (TTL) to generate the CLK input.
The high speed logic must also generate the timing and control signals necessary for the shift register, latch, and MUX control. The processor communicates with the CRT controller through an eight - bit data bus by reading or writing into the 19 registers. The refresh memory address is multiplexed between the processor and the CRT controller. Data appears on a secondary bus separate from the processor's bus. The secondary data bus concept in no way precludes using the refresh RAM for other purposes. It looks like any other RAM to the processor. A number of approaches are possible for solving contentions for the refresh **memory.**

1. Processor always gets priority. (generally, " hash " occurs as ECPU68K and CRT controller clocks are not synchronised.)

2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizonal and vertical retrace times.

3. Synchronize the processor with memory wait cycles (states).

4. Synchronize the processor to the character rate as shown in figure 4.

The ECRT - board makes use of solution 3.

FIGURE 10 – TRANSPARENT REFRESH MEMORY CONFIGURATION TIMING USING M6800 FAMILY MPU

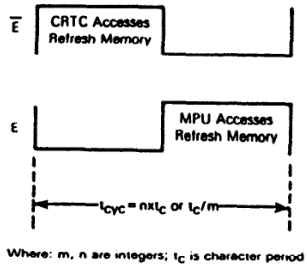


figure 4.

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Sheet 3 of schematic 7092E9311-65

We can split sheet 3 into two parts:

- timing circuitry
- bus connection circuitry

Bus connection part.

As we start on the left side of the sheet, we see that the ECRT data bus and the ECRT address bus are separated from the ECPU68K bus system by tri-state buffers (G9,F9 and E9).
Because the ECPU68K has control over the system all the time, the direction and the enable lines of the address bus (F9, E9) pin 1 and 19, are permanently low.
The control bus goes in to PAL B9. This PAL generates signals which are necessary to communicate with certain parts of the ECRT board.

At the bottom of the sheet we see that the data bus is connected to a register 19. This makes It possible for the CPU to write down a byte that contains information about the chosen character set, and in which RAM bank the CRT controller is working. This configuration enables the ECPU68K to disregard the mode in which the system works. The ECPU68K is able to check this mode any time by generating a /REGRD. The data is then available on the data bus (via H9). To write in register (19) the ECPU68K generates a /REGWR, and the data on the data bus is latched into the register. By reading H9, the ECPU68K also detects the presence of the ECRT-board (bit D3 is low) and the power-line frequency. (bit D7 is low for 60Hz and high for 50 Hz).

/CPUREQ is latched into a D-FF (D8). It is latched into the FF by the CHARCLK. The output is called /CPUGTD. This signal plays an important *role* in the communication between the ECPU68K and ECRT board.

In the middle of the sheet we see an oscillator. The output goes into a D-FF (A8), which divides the frequency by 2. We now obtain the dot clock (12.5MHz). The output of the D-FF goes Into another D-FF, which also devides by 2. We now obtain the DOTCLK6. At the end we have a frequency of 6.25 Mhz. This frequency goes into a counter (F8), which counts from 7 to F. This counter drives two PAL's, which take care of the timing of the board.

At the top of the sheet we see three D-FF (I8,J8).
These FF are used to synchronize the signals DE and PRENBAR, which are used for the BAR option.

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Sheet 4 of schematic 7092E9311-65

This sheet contains the heart of the ECRT-board. As we start at the left side of the sheet we see the CRT controller J5. This chip has input and output lines. Input lines are:

1	data bus	DO . . . D7
2.	Enable line	E
3.	Chip select	/CSCRTC
4.	Read/Write line	R/W
5.	Reset	/Reset
6.	Light strobe	LPSTB
7.	Clock	CHARCLK
8.	Register select	Al

Output lines are:

1.	Memory address lines	MA0 . . . MA11 (MA12-MA13 not used)
2.	Row address lines	RA0 . . . RA4
3.	Horizontal sync.	HS
4.	Vertical sync.	VS
5.	Cursor	
6.	Display enable	DE
7.	Data bus	DO . . . D7

The nineteen registers of the CRT controller may be accessed through the data bus. Only two memory locations are required as one location is used as a pointer to address one of the remaining eighteen registers. These registers take care of the following functions:

- control horizontal and vertical timing
- interlace or non-interlace operation
- row address and memory address operation
- define the cursor
- cursor address
- start address
- light pen register
- sync pulse (horizontal and vertical) timing

There are three different busses to the ECRT-board:

- address bus
- data bus
- control bus

This implies that there is another component which has access to the board. This component is the ECPU68K. The ECPU68K is able to communicate with the CRT controller and the RAM (G3). Selection of ECPU68K- RAM access is made possible by switching the address bus. This is done by three multiplexers (I5,I4,I3). When the signal /CPUACC is low, the ECPU68K has access to the RAM (G3) address lines (e.g. to write a new text page in it). When the signal /CPUACC is high, the CRT controller (6845) has access to the RAM.

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The ECPU68K data bus is seperated from the RAM (G3) data bus by tri-state buffer (D2). When the signal /ENCPUD is low the ECPU68K can read or write data from/to RAM, When the signal /ENCPUD is high the ECPU68K data bus is disconnected from the RAM.

Data on the RAM data bus (VDO . . . VD7) is latched into latch D3 by CHARCLK. Outputs of D3 are LVDO . . . LVD7. LVDO . . . LVD6 point to a character in the EPROM (D5), while RAO . . . RA3 point to a specific line of the character involved. The output of the character generator (D5) represents the parallel pixel data . (PDO . . . PD7). The pixel data is loaded into C6 by /LDSR. Data is serial shifted out by DOTCLK.

To take care of the time delay between the moment that outputs of the 6845 are activated and the moment the data appears at the output of the shift register (C6), synchronisation of signals DE and CURSOR is obtained by D-FF I2,

With signals RAMBSELO-RAMBSEL2 a "text page" in the RAM (G3) can be chosen. There are 8 pages possible when a 32K*8 RAM is used. In case of a 8K*8 RAM there are 2 pages possible. The ECRT board is standard delivered with 8K*8 RAM.

With signals CHSO-CHS2 a "character set" can be chosen in the EPROM (e.g. Hebrew). There are in total 8 sets possible.

The signal INV is used as a gate signal for LVD6. When INV is high and LVD6 is high an inverted character is addressed in the EPROM.
The signal CHARINV is connected to the serial input of the shift register (C6) to prevent a "blank space" between two inverted characters, If a "blank space" is desired jumper W5 must be set to 1-2 position. In this case jumper W4 may be also in 1-2 position.

The signal LVD7 can be tied to A15 of the EPROM (27512 only) via jumper W3. This opens the way for future features. This is not supported by software at the moment.

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sheet 5 of schematic 7092E9311-59

Because the ECRT-board should be compatible with the old board, many D-FF are necessary to obtain this compatibility. Options which where available are:

- Blinking of characters
- Inverting of characters
- Bar graph

How is the difference made between a normal character, and an inverse character ?

A byte consists of eight bits. Using two bits (LVD 6 and LVD7), we are able to detect how the character should be displayed. This implies that we have to scan these two bits for every raster and / or character. This is done by D-FF (A5,A6).These two Flipflops are clocked by the signal CHARO.0.

To make blinking possible an oscillator (A7) takes care of the blinking rate. Blinking is synchronized with the vertical sync by D-FF A6.

The first character of a frame (characterO.0) determines if options are allowed. This means that this character has to be checked every frame, to see if blinking or inverse option is enabled. Bit 6 and bit 7 of characterO.0 contain this information.

Character 0.0	bit 7	bit 6	frame options
	0	0	**no** option
	0	1	blinking
	1	0	inverse
	1	1	blinking and Inverse

Bit 6 of a random character (not characterO.0) determines if the options are on or off for the character Involved. Scanning is done by D-FF A3 (clocked by SYNDECU). If bit 6 is "1" then the options defined by character 0.0 are on.

To make it possible to display a bargraph, the length of the bar should be available. Bit 7 of the first character of a line is scanned to see If a bargraph is required. (No bargraph possible on the first line of a frame) If bit 7 is "1", a bargraph is required, In that case the rest of the character bits do not present a character but the length of the bargraph. Scanning of bit 7 is done by D-FF A3 which is clocked by signal /CLRBARCTR.
The length of the bargraph (bit0-bit6) is loaded into A2 and A3 by signal /LDBAR. These counters count up each time that BARCLK' (3.125MHz) goes high. When count FF is reached, the next count 00 makes signal BARDATA low. This stops (via PAL H8 and signal CLRBARCTR) the BARCLK. So BARDATA remains low.
Maximum length of bar: 8Ohex must be loaded.
minimum length of bar: FChex must be loaded.
The signals /CLRBARCTR, PRENBAR and ENBAR take care that the bargraph starts at the proper position. These signals are generated on sheet 3 of the schematic.

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VIDEO PAL (C7) combines all the signals, and the output /DIGVIDEO is the correct signal to control the CRT beam. Because there is a possibility to use composite video, the HS and VS are added together (D8,E8), and added together with /DIGVIDEO. Transistor T1 delivers the composite video. Because there is a digital scope board (MCS 2000) which needs also a HS and VS, we need to delay these signals to be able to overlay the text video (from ECRT board) exactly on the scope video signal. This delay is generated by E6 and F6.

Jumper W6 and W7 make it possible to make a choice to have pos. or neg. synchronisation signals.

Interaction ECPU68K & ECRT board [CPUREQ].

For the next pages we use the abbriviation TC, which stands for Timing Chart.

Because the ECRT board is not able to work completely stand alone, it is necessary to communicate with the ECPU68K. Because the ECPU68K is the only one who has full control of the system, the ECPU68K is responsible for sending information to the boards. For this communication the ECPU68K has three different busses. Available are:

- address bus
- data bus
- control bus

To select a board, and on this board a specific component the ECPU68K uses the address bus to indicate its intention. To be able to send or receive information he uses its data bus. To make sure no information gets lost, control signals are sent and received by using the control bus. As explaned before, the CRT controller (6845) is continuously scanning Its screen memory to fill the screen with the latest data. Its interaction with RAM (G3) occurs at specific moments. The ECPU68K hae access to the RAM (G3) after video data (VD) is latched into D3 until the CRT controller (6845) sets up the address (MA) for the next character. This means that the ECPU68K has access to the RAM during the high period of the signal CHARCLK (960 ns).
Other components accessible for the CPU are:

- CRT controller (6845)
- Buffer H9
- Register 19

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CPUREQ

To indicate the intention for communication the ECPU68K places a /CPUREQ on the control bus of the ECRT board. /CPUREQ is an output signal of PAL B9, and it is activated when the following formula is true:

```
CPUREQ  := MEMRD * BLDS it MEMEN * BA 21 *  /RESET
         + MEMWR  * BLDS * MEMEN * BA 21 *  /RESET
```

- MEMRD : memory read

  This signal comes from the ECPU68K, and indicates a memory read action. This signal is true If we want to read from 000000(H) - 3FFFFF(H)

- MEMWR : memory write

  This signal comes from the ECPU68K, and indicates a memory write action. This signal is true if we want to write to 000000(H) - 3FFFFF(H)

-BLDS : buffered lower data strobe

  This signal indicates that the lower eight data bits are active. DO . . D7

-MEMEN : memory enable

  This signal is a buffered address strobe, and indicates that the value on the address bus is valid.

- BA 21 : buffered address 21

  This signal reduces the memory map. CPUREQ becomes now active in the area 200000(H) - 3FFFFF(H)

The formula Indicates that CPUREQ gets activated by a READ action as well as a write action, to this specific area.

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Interaction confirmed. [CPUGTD]

For the following description, we refer to the TC and sheet 3 of the schematic.

When a /CPUREQ has been generated, it may be possible that access is not allowed. The CPU has to wait the time between the request and /CPUGTD. This is done by Introducing wait cycles. The ECPU68K needs for executing an Instruction eight cycles, -SO . . . S7-. When the ECRT-board receives an /CPUREQ, it makes the READY line low. This signal forces the ECPU68K to stop, and to introduce WAIT cycles. When the ECRT board confirms the /CPUREQ, it makes the READY line high. The ECPU68K is now able to continue Its communication. The signal /CPUREQ is translated into /CPUGTD by triggering on the rising edge of CHARCLK. This is the procedure which has to be taken by the ECRT everytime the CPU wants to communicate with one of the components at the ECRT-board. What kind of communication configurations are possible ?

We have four components to communicate with.

- CRT controller (6845)
- RAM (G3)
- Register 19
- Buffer H9

That results in seven different operations, where there are six controlled by ECPU68K:

- ECPU68K writes to CRT controller (6845)
- ECPU68K reads from CRT controller
- ECPU68K writes to RAM (G3)
- ECPU68K reads from RAM (G3)
- CRT controller (6845) reads from RAM (G3)
- ECPU68K writes to register I9
- ECPU68K reads from buffer H9

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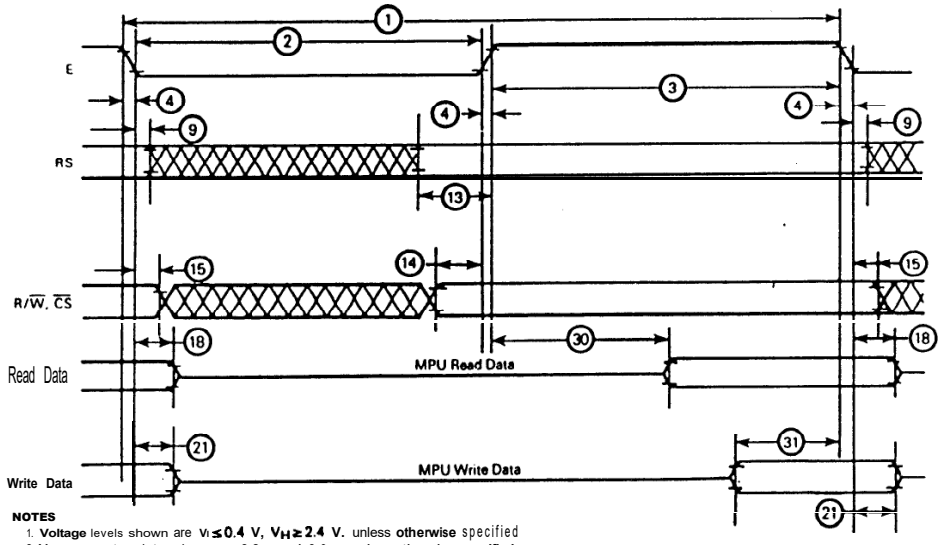
Timing CRT controller. (6845)

BUS TIMING CHARACTERISTICS (See Notes 1 and 2) (Reference Figures 3 and 41

Ident. Number	Characteristic	Symbol	MC6845 MC6845 ☆ 1		MC68A45 MC68A45 ☆ 1		MC68B45 MC68B45 ☆ 1		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time (RS)	t_{AH}	10	–	10	–	10	–	ns
13	RS Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	R/W and CS Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	R/W and CS Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Peripheral Output Data Delay Time	t_{DDR}	–	290	–	180	0	150	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	–	80	-	60	-	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR} max (high impedance).

MC6845 **BUS TIMING**



NOTES
1. Voltage levels shown are $V_l \leq 0.4$ V, $V_H \geq 2.4$ V. unless otherwise specified
2 Measurement, points shown 0.8 v and 2.0 v. unless otherwise specified

Figure 5. Timing chart, CRT controller (6845)

Looking at the chart we distinguish six different signals.

- E
- RS
- R/W
- /CS
- Read data
- Write data

The most important signal is the E signal. The TC gives us information about the **time** relation between the E signal and the other signals. How must we conceive this chart ?

(Note: the ECRT-board contains a 2MHz version of the 6845, but a 1.5MHz (MOTOROLA) version will do also. (not a 1MHz version!!))

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See fig. 5. (timing is related to middle column)

- RS (address A1)

  This signal should be available at least 60 ns earlier than the rising edge of E, and must be available for at least 10 ns after the falling edge of E.

- R/W and /CS

  These signals should be both available, at least 60 ns earlier than the the rising edge of E, and must be available for at least 10 ns after the falling edge of E.

- Write data

  The data should be available, at least 80 ns earlier than the falling edge of E, and must be available for at least 10 ns after the falling edge of E.

If the communication has to take place, we have to obey these demands.

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ECPU68K writes to CRT controller.

See timing chart

If we want to write to the CRT controller, some signals need to be generated. To get access to the CRT controller, we need to generate a signal to select this chip. This is done by generating a /CSCRTC. When will there be a /CSCRTC? According to the formula:

/CSCRTC := CPUREQ * BA 16 * /A15 * CPUGTD * CHARCLK

This signal is true everytime BA 16 and /A15 are active, and there is a CPUREQ. To synchronise the CPU with the CRT-board the CHARCLK and CPUGTD are used. Communication has to take place according to the timing chart of the 6845

The write action,

How does the communication takes place on the board?.

For the next story we refer to TC of 6845.

We know how to get access to the board. We start at the beginning of the CHARCLK cycle (number 7). The time between 7 and A, is the time that the CRT controller is allowed to communicate with the RAN. The CPU has access to CRT controller during intervals A to end of F.

At the rising edge of CHARCLK, /CPUGTD and /CSCRTC are generated.

/CSCRTC = CPUREQ * BA 16 * /A15 + CPUGTD * CHARCLK

We have to wait till READY becomes high.

```
READY = MEMRD * BLDS * MEMEN it BA 21 +  /CPUGTD   1.
      + MEMWR * BLDS * MEMEN it BA 21 * /CPUGTD    2.
      + WAIT                                       3.
```

Terms 1 and 2 keep READY low from beginning of CPUREQ to beginning of CPUGTD. TERM 3 KEEPS ready low from beginning of CPUGTD until WAIT goes low.

If we want to write to the CRT controller we have to bear in mind that the ECPU68K generates CPUREQ for a write action. This means it already has its data available, it has also set its R/W line in write position. The data will be removed from the bus, one ECPU68K clock cycle later, after the moment that the ECPU68K detects a /DTACK. /DTACK is true at the moment that the READY line is high. Detection of /DTACK takes place at the falling edge of the ECPU68K clock cycle 4.

(P.S./DTACK is the ECPU68K data acknowledge input.)

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How are the times related to the E signal?

- RS (address A1)

  RS is activated by address line A1. This line is available at the moment a CPUREQ, is generated. The minimum time that A1 is available (before positive going of E) is more than 160 ns. This long enough for good functioning.

- /CS and R/W

  R/W is available at the moment the CPUREQ, is generated. /CS is available at the rising edge of CHARCLK. This is 160 ns. before E goes positive.

- Data is available at the moment the CPUREQ is generated. The minimum time (before E goes positive) is more than 160 ns.

To be sure that the timing of the CRT controller is obeyed, we make the high period of E smaller during a ECPU68K write action to the CRT controller.

```
E := Qd * QC * Qb * /Qa *  /READ * CPUGTD * /CPUACC
   + Qc * Qb * Qa
   + Qd * /QC * /Qb
   + Qd * /QC * Qb  */Qa
```

On the falling edge of E the data is clocked Into the CTR controller. We saw that the signals and data should be available some time after the falling edge of E. We have two possible situations

- Worst case
- Best case

Worst case:

The worst case is that READY changes just after the falling edge of the ECPU68K clock. This means that the /DTACK is seen 250 ns later, and that the CPUREQ will be removed from the bus 250 ns (minimal) after DTACK was seen. (500 ns after READY)

Best case:

The best case is that READY becomes high just before the falling edge of the ECPU68K clock. This means that /DTACK takes place just after the moment that READY becomes high. This has a result that the CPUREQ will be removed from the bus (minimal) 250 ns later, after detection of DTACK.

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For both the best and worst cases, CHARCLK takes care that ECPU68K access to the ECRT-board is stopped before a display cycle (low period of CHARCLK) is started. Normally ECPU68K access is finished before a new display cycle is started. But when the ECPU68K does not remove his CPUREQ, CHARCLK takes care that CPUGTD is removed at the begin of a new display cycle.

In both cases the minimum time that signals should be available is achieved.

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CPU reads data from CRT controller.

See timing chart

The ECPU68K gets access to the ECRT-board by the action described on pages 13 and 14.

Reading Information out of the CRT controller takes more time than writing. This is because the ECPU68K has to clock the data into its buffer. It has to get the data bus out of tri-state. We have to bear In mind that by a read action, the ECPU68K has already determined its R/W line in read **mode.**

To make sure everything runs smoothly, timing has to be obeyed.

What should the timing look like?.

It will cost the CRT controller at least 180 ns after the rising edge of E, to have the data available on the data bus, end it will stay available 20 ns after the falling edge of E.
All other signals have the same timing es described in Timing CRT controller.

The read action.

For the following story we refer to TC 6845.

We know how to get access to the board. We start at the beginning of the CHARCLK cycle (number 7). The time between 7 and A, is the time that the CRT controller is allowed to communicate with the RAM.
The ECPU68K is allowed to generate a /CPUREQ all the time. At the rising edge of CHARCLK we derive a /CPUGTD. At this same moment /CSCRTC is generated.

```
/CSCRTC := CPUREQ * BA 16 * /A15 * CPUGTD * CHARCLK
```

We have to wait till READY becomes high.

```
READY = MEMRD * BLDS it MEMEN * BA 21 *  /CPUGTD   1 .
      + MEMWR * BLDS * MEMEN * BA 21 * /CPUGTD    2.
      + WAIT                                      3.
```

Terms 1 and 2 keep READY low from beginning of CPUREQ to beginning of CPUGTD. Term 3 keeps READY low from beginning of CPUGTD until WAIT goes low.

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```
WAIT   = CPUREQ * /CPUGTD                          1.
       + CPUREQ * WAITF                            2.
       + WAIT * /E * CPUGTD                        3.
       + /READ * WAIT  * Qa * Qb */QC * Qd         4.
       + /READ * WAIT *  DOTCLK6                   5.
```

terms 1 and 2 makes WAIT active from the start of CPUREQ, till the start of CPUGTD. Terms 3, 4 and 5 are time dependent and generated by the internal timing.

The moment that READY becomes high determines the time necessary for the CPU to read the data. This read action takes place one ECPU68K clock cycle later than the moment /DTACK becomes active. /DTACK becomes active at the falling edge of the ECPU68K clock cycle, when READY is high. We have two limits:

- Worst case
- Best case

Worst case:

The worst case is that READY changes just after the falling edge of the ECPU68K clock. This means that the /DTACK takes place 250 ns later, and that the data wil be clocked in 500ns. After this the ECPU68K will remove the CPUREQ.

Best case:

The best case is that READY becomes high just before the falling edge of the ECPU68K clock. This means that /DTACK takes place just after the moment that READY becomes high. This has as result that the data will be clocked in 250 ns later than /DTACK. After this the ECPU68K will remove the CPUREQ.

For both the best and worst case, CHARCLK takes care that ECPU68K access to the ECRT-board is stopped before a display cycle (low period of CHARCLK) is started. Normally ECPU68K access is finished before a new display cycle.

In both cases the minimum time that signals should be available is achieved.

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General RAM access.

Because both the ECPU68K and the CRT controller must have access to RAM, is it necessary to control the access time.

The RAM chip contains:

- address bus
- data bus
- control bus

Looking at sheet 4 of schematic we see that the MA lines of the CRT controller take care of determining the address in RAM.
The multiplexer I3,I4 and I5 determine which has control of the the address bus, the ECPU68K or the CRT controller.
Selection between ECPU68K and CRT controller is accomplished by the signal /CPUACC.

```
CPUACC = CPUREQ * /BA16 * CPUGTD * CHARCLK        1.
       + CPUACC * E                               2.
```

Term 1. takes care of the selection and a part of the timing, and is active from 200001(H) - 20FFFF(H).

Term 2. takes care for the timing to insure that the multiplexers remain selected after the ECRT is ready with its job.
RAM data selected by the CRT controller is latched into the D-latch D3. The data bus buffer D2, is enabled by /ENCPUD

```
/ENCPUD := Qa * Qb * /QC * Qd *  CPUACC
         + /QB * QC it QD * CPUACC
         + /Qa * Qb * Qc * Qd *  CPUACC
```

The selection takes place at certain moments, depending on the value of counter (F8), and if CPUACC is available. The direction of the data buffer D2, depends on the value of R/W.
The choice R/W is made at the moment that the ECPU68K generates a CPUREQ. What is left to be done is to determine the level of control signals:

- /CSRAM
- /OERAM
- /WRRAM

```
CSRAM  := /Qb * /QC it Qd
        + /Qa * Qb * /QC * Qd
        + CPUGTD * CPUACC + Qa * Qb * /QC * Qd *  CPUREQ
        + CPUGTD * CPUACC * /Qb * Qc * Qd it CPUREQ
        + CPUGTD * CPUACC * /Qa * Qb * Qc * Qd *  CPUREQ


OERAM  := Qa * /Qb * /QC * Qd
        + READ * CPUREQ * CPUGTD * CPUACC * Qa * Qb * /QC * Qd
        + READ * CPUREQ * CPUGTD * CPUACC it /Qb it Qc * Qd
        + READ * CPUREQ * CPUGTD * CPUACC + /Qa * Qb * Qc * Qd
```

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WRRAM := Qa * /Qb * /QC * Qd * /READ * ENCPUD * CPUACC * CPUGTD
* CPUREQ

CSRAM'is true at the ECRT clock cycles: 8 . . . E

OERAM is true at the ECRT clock cycles: 9 and B . . . E

WRRAM is true at the ECRT clock cycle : D

If we want to communicate with the RAM we have to initialize these signals, and take care of the timing charts.

RAMBSELO - RAMBSEL2, determine in which RAM page we are working, and is determined by the value written In the register I9.

There are two possibilities:

- writing to RAM
- reading from RAM

The write or read action can only be succesful If the timing chart of the RAM is obeyed. The minimum time to obtain a read or write cycle is 120 ns. This is the only time they have in common.

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Writing to RAM by CPU.

See timing chart

According to the timing chart we have to supply the following signals, to enable a write action.

- Addresses
- /CSRAM
- /WRRAM
- Data in

A write action occurs during overlap of a low /CSRAM and a low /WRRAM.

As we see in the general TC, it appears that /CSRAM is available earlier than /WRRAM. The crucial point is the write action.

Write Cycle

Parameter	Symbol	μPD43256C/GU -10L		μPD43256C/GU -12L		μPD43256C/GU -15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	100		120		150		ns
Chip Select to End of Write	tCW	80		85		100		ns
Address Valid to End of Write	tAW	80		85		100		ns
Address Set-up Time	tAS	0		0		0		ns
Write Pulse Widlh	twp	70		70		90		ns
Write Recovery Time	tWR	5		5		5		ns
Data Valid lo End of Write	tDW	40		50		60		ns
Data Hold Time	tDH	0		0		0		ns
Write Enable to Output in HZ	twHz		35		40		50	ns
Output Active trom End of Write	tow	10		10		10		ns

Write Cycle No. 2 (/CS Controlled)(1)(2)

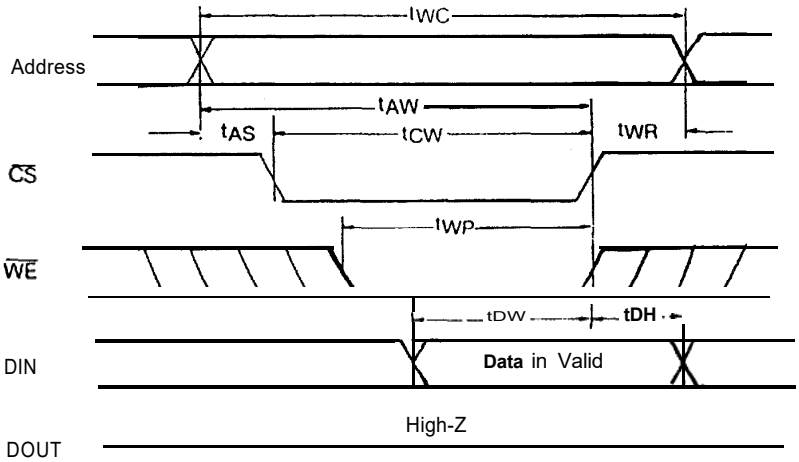


Figure 6.

Notes (1) a write occurs during the overlap of a low /Cs and a tow /WE.
(2) /CS or /WE must be high during address transition.
(3) If /OE is high. I/O pins remain in a high impedance state.
(4) During this period I/O pins are in the output slate, therelore the input signals of opposite phase to the oulputs must not be applied.

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The TC tells us that : (120 ns RAM is used)

The address, should be available 85 ns before the falling edge of /CSRAM.

/CSRAM, should be available 85 ns before the rising edge of /WE

The minimum time that /WRRAM should be low is 70 ns.

The data should be available 50 ns before the falling edge of /WE.

How does the write action take place at the ECRT-board ?

We must bear in mind that it is the ECPU68K that wants to write. This means that at the moment that It generates a CPUREQ, the data is available on the data bus, and that the R/W line is in write mode.

The write action.

/CSRAM gets low every time the counter has the value 8 or 9 or A. After the low period the line will go high. But in case of a write action or read action it will stay low.
/OERAM gets low every time the counter has reached the value 9. Then it goes high again. But in case of a read action it will stay low.

/WRRAM gets low only one clock cycle: the cycle from D to E.

When /CPUGTD comes through, /CPUACC gets active. After a while the READY line gets high. Because the /WRRAM gets low at specific moments, it is important to see when the CPU receives a /DTACK. There are two possible situations:

- Worst case
- Best case

Worst case:

The worst case is that READY changes just after the falling edge of the ECPU68K clock. This means that the /DTACK takes place 250 ns later, and that the CPUREQ will be removed from the bus +/- 500 ns later.

Best case:

the best case is that READY becomes high just before the falling edge of the ECPU68K clock. This means that /DTACK takes place just after the moment that READY becomes high. This has as result that the CPUREQ will be removed from the bus 250 ns later, after detection of DTACK.
In all cases, ECPU68K - RAM access is finished before the CRT controller wants to communicate with RAM.
For Both the best and worst cases, CHARCLK takes care that CPU access to the ECRT board is stopped before a display cycle (low period of CHARCLK) is started. Normally CPU access is finished before a new display cycle.

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CPU reads from RAM.

See timing chart.

This situation is not used at the moment.

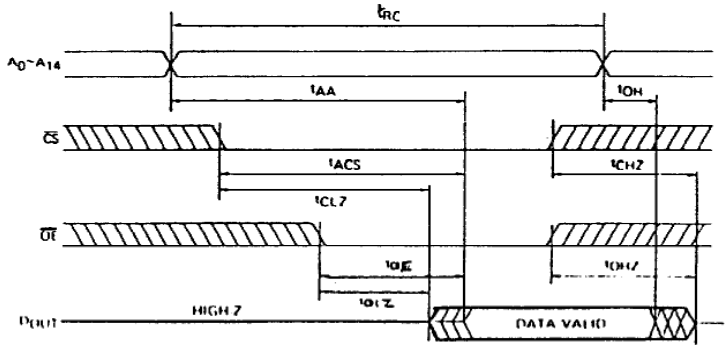
The signals needed for an read cycle are:

- addresses
- /CSRAM
- /OERAM
- Data

READ CYCLE

Parameter	Symbol	µPD43256C/GU -10L		µPD43256C/GU -12L		µPD43256C/GU -15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Chip Select Access Time	t_{ACS}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		50		60		70	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output In Low Z	t_{CLZ}	10		10		10		ns
Output Enable to Output In LZ	t_{OLZ}	5		5		5		ns
Chip select to Output in HZ	t_{CHZ}		35		40		50	ns
Output Enable to Output in HZ	t_{OHZ}		35		40		50	ns

READ CYCLE TIMING CHART [1].[2]. [3]



Notes [1] WE is high for read cycle.
[2] Device is continuously selected, CS = OE = V_{IL}.
[3] Address valid prior to or coincident with CS transition low.

figure 7.

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The minimum time to obtain the data is 120ns after the set up of the address,

The minimum time /CSRAM should be low before data is valid is 120 ns.

The minimum time /OERAM should be low before data is valid is 60 ns.

The read action

It starts when /CSRAM becomes low. If there was a CPUREQ for a read action, CPUGTD gets low at the rising edge of CHARCLK. /OERAM gets low when the counter has reached B. At this time READY becomes high. When READY is high /DTACK determines the moment of the ECPU68K to clock in the data. There are two possible situations.

- Worst case
- Best case

Worst case:

The worst case is that READY changes just after the falling edge of the ECPU68K clock. This means that the /DTACK takes place 250 ns later, and that the data will be clocked In 500ns. After this the ECPU68K will remove the CPUREQ.

Best case:

The best case is that READY becomes high just before the falling edge of the ECPU68K clock. This means that /DTACK takes place just after the moment that READY becomes high. This has a result that the data will be clocked in 250 ns later than /DTACK. After this the ECPU68K will remove the CPUREQ.

For both the best and worst case, CHARCLK takes care that ECPU68K access to the ECRT board is stopped before a display cycle (low period of CHARCLK) is started. Normally ECPU68K access is finished before a new display cycle.

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Read action by CRT controller.

See timing chart.

The CRT controller can only point to an address in RAM in which is located (in ASCII code) the next byte to be displayed. The MA lines keep track of the character that should be displayed, end the RA lines keep track of which line of the character should be displayed.

It takes eight DOTCLK6 clock cycles to display a character (line). After these eight cycles a new character should be fetched. During the time that is necessary to fetch a new character, the CHARCLK is low. During this time the CRT controller (6845) is allowed to communicate with RAM. To keep this communication time as brief as possible, the data of the address addressed by the CRT controller, is latched Into a D-latch D3. By doing so, time is obtained for the ECPU68K to communicate with RAM. After the falling edge of CHARCLK it will take 160 ns (maximum) to have the new MA and RA lines available. To have other signals as:

- HS
- vs
- DE

ready, will take 300 ns (maximum).

To have data available at the data bus of the RAM, we have to obey the TC of the RAM. Lines necessary to obtain data are:

- /CSRAM
- /OERAM
- address

/CSRAM has to be 120 ns (minimum) available before data is valid.

/OERAM has to be 60 ns(minimum) available before data is valid.

This action has to be taken **every time** a new character is needed. The data flow is automatically obtained by the internal timing. How is this achieved on the ECRT board ?.

At the falling edge of CHARCLK, the MA and RA addresses will change. During the time that CHARCLK is low, the board has time to generate the new video data (VD) at the RAM output **lines.**

The time from 7 to 8 is used to change the MA and RA addresses
The time from 8 to A /CSRAM is made active.
The time from 9 to A /OERAM is made active.

The data available at time A, is latched into D-latch D3.
If we take a look at the TC, we see how the timing between certain signals is obtained.

HA & RA lines are stable at time 8
Data is valid at time 9 (VD).
LVD is available just after the rising edge of CHARCLK.

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Display set up.

The screen consists of 512 characters. These characters have their own place in RAM **memory.** The places on the screen corresponding with the places in RAM are:

	Seen from ECPU68K.	Seen from CRT controller (6845)
A :	202401(H)	0200(H) (characterO.0)
B :	20243F(H)	**021F(H)**
C :	2027C1(H)	03EO(H)
D :	2027FF(H)	03FF(H)

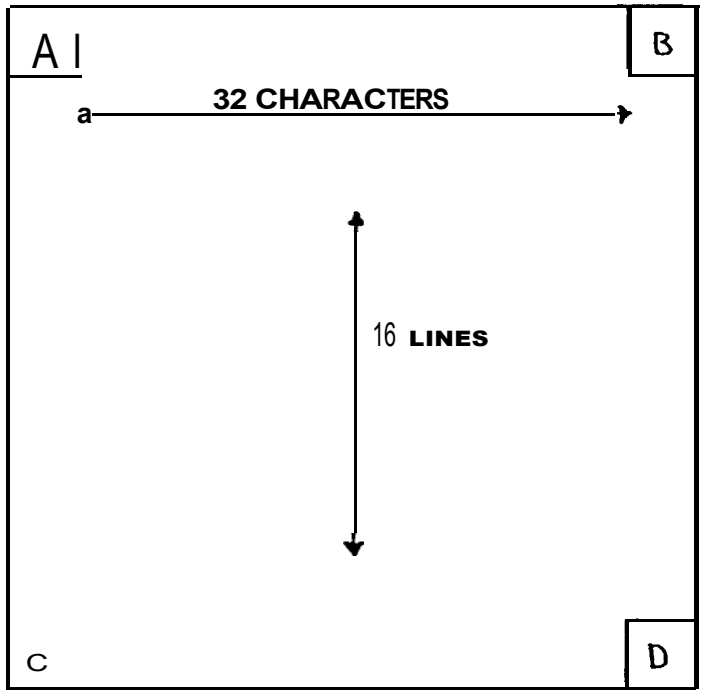


Figure. 8.

The CRT screen is filled with lines. The total amount of lines is determined by the ECRT board. Because this board had to be compatible with the old board, the same amount of lines are used. In the old situation each line was 64 us long. This means a horizontal frequency of 15625 Hz. Because we have 16 character rows, and each character row is built up out of 15 lines, we obtain 240 lines. In total there are 312.5 lines (20ms divided **by** 64 us). This leaves us with 71.5 lines. A vertical sync, is 3 lines wide, and there are 30 lines available between the **bottom** .of the screen and the last character line. This results in having 39.5 lines left. These are between the vertical sync and the first character line. see figure 9.

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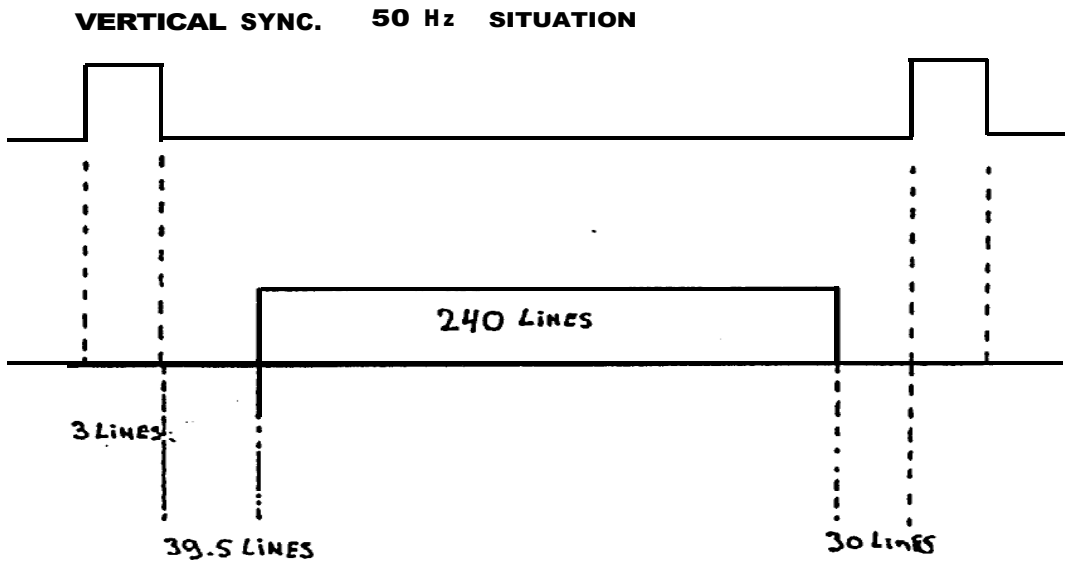


figure 9.

This is only in the 50 Hz situation. In the 60 Hz situation we have the screen set up as shown in figure 10. Because the frequency is higher, there are fewer lines available. We have available 260 lines. (16.66 ns divided by 64 us).

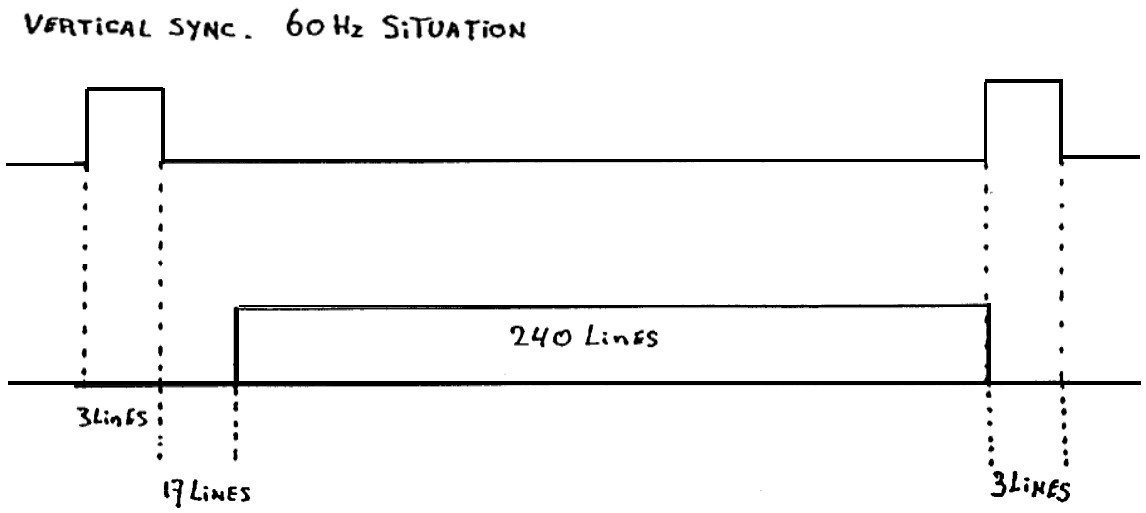


figure 10.

When a cursor crosses the screen, text standing on the screen is still readable. You can read through the cursor because of the ex-or function. The software however does not use the cursor feature of the CRT controller. Instead of a cursor an inverted space character is displayed.

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Character set up.

See appendix A.

A character consists of dots which form a matrix. See figure 11. We use a matrix of 16 dots wide and 15 dots high. To obtain space between the characters, not all the dots are used. We obtain a matrix in 8 matrix.

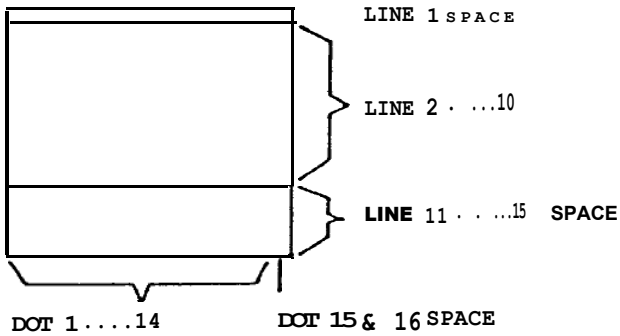


figure 11.

When the data is latched into D-latch D3, the character generator is enabled to produce the character information. It does this by sending bytes to the parallel to serial converter, when /OECHARGEN is active.

/OECHARGEN := Qc * Qb * Qa + Qd * /QC * Qb * Qa + Qd * Qc * /Qb * /Qa

This signal is active B, C, F and 7

To obtain one character line the character generator has to send two times one byte to the converter. How doee this work on the board ?. When we look at the TC, we see that the selection SEL R/L is low at the moment a new character is fetched. At time D, during the display action the SEL R/L is made high,

SEL R/L := Qd * /QC * Qb + Qd * Qc * /Qb * /Qa

High from D . . . 9

So selection is made before the new byte if available.
The date are clocked out at the DOTCLK rate,

If we take a look at the CD signal, we see that during the read action of the CRT controller, the shift register still contains information, of the previous character, At the time the new ASCII code is available, it still has to clock out 4 dots. After the latest shift action the new byte is parallel loaded by LDSR.

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Options.

Just as the old CRT board, the ECRT board also has options. There are three options available:

- Blinking
- Inverting
- Bar graph

How are these options recognized. The options blinking and inverting are available per frame, This means that everytime we start a new frame we have to initialise a part of the board, to allow options. This initialisation takes place by determining the value of two bits. We have one byte available to represent a character. One byte consists of eight bits. We use only 6 bits for the character. This means we have 64 different characters available, Bit 6 and bit 7 are used to allow options.

bit 6	bit7	option
0	0	non
0	1	blinking
1	0	inverting
1	1	inverting & blinking

Only the first character of a frame contains this Information. Other characters only use bit 6 to indicate that an option for that specific character is wanted. Bit 7 of this character is don't care.

How do we indicate that a bargraph is wanted ?

For this option we have to look at the first character of each text row. This character sets bit 7 to indicate that a bar is wanted. Bit 0 to 6 are used to represent the length of the bar.

DESYN clocks a D-FF A5 (sheet 5), so every time there is a new line a logic " 1 " is clocked in. At a VS, the FF (A5) is cleared. The output clocks two D-FF (A5,A6). The Inputs are LVD6 respectively and LVD 7. The output tells the VIDEO PAL if options blinking or invert are allowed. The output INV of A9 goes to the character generator to choose the inverted values(this is done by choosing another memory map) of the wanted character.

The blinking rate is obtained by an oscillator A7. The most important D-FF is A3. This FF keeps track of bit LVD6 (for every new character that should be displayed) to see if there is an option wanted. LVD6 is clocked by SYNDECU, this signal runs at the character rate.

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Bar option.

The bargraph is **also** an option available on the board. To see if a bar&graph or a character should be displayed, the first character of a new text row is tested. If bit 7 of that character is true then the value of bit 0 . . . bit 6, represent the length of the bar. If it is a bargraph, then the first character is not displayed. The length of the bargraph is obtained from the bit value (bit0 . . . bit6). If the first character of a new row, indicates a bar, then that byte is loaded into the counters A2 and Al. Because bit seven is included we have always an offset. The counters are counting from 80(H) . . . FF(H). The largest value that we may fill in is FC. The count rate is determined by the speed at which BARCLK runs. We use ENBAR to take care that the first character is not displayed. ENBAR is generated in FF J8. The FF is clocked by CHARCLK.

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Signal abbreviations

A1-A15	=	Address lines (on ECRT board)
BA1-BA21	=	Buffered address lines (on backplane)
BARCLK	=	Bargraph clock
BARDATA	=	Bargraph date
BD0-BD7	=	Buffered data lines (on backplane)
BIT7CH0	=	Bit 7 of character 0 (first char. of a line)
BLDS	=	Buffered lower data strobe
BLINK	=	Blink
BLINKEN	=	Blink enable
BR/W	=	Buffered reed / write
CD	=	Clocked data (serial)
CHARO.0	=	Character 0.0 (first char. of a frame)
CHARCLK	=	Character clock
CHARINV	=	Character Invert
CHSO-CHS2	=	Character set
CLRBARCTR	=	Clear bargraph counter
CLRSR	=	Clear shift register
COMP VIDEO	=	Composite video
CPU	=	Central processing unit
CPUACC	=	CPU access
CPUGTD	=	CPU granted
CPUREQ	=	Central processing unit request
CSCRTC	=	Chip select cathode ray tube controller
CSRAM	=	Chip select random access memory
CUSYN	=	Cursor synchronised
DO-D7	=	Data lines (on ECRT board)
DE	=	Display enable
DESYN	=	Display enable synchronised
DIGVIDEO	=	Digital video
DOTCLK	=	Dot clock (12.5 MHz)
DOTCLK6	=	Dot clock (6.25 MHz)
E	=	Enable
ECRT	=	Enhanced cathode ray tube (board)
ECRTSEL	=	ECRT select
ENBAR	=	Enable bargraph
ENCPUD	=	Enable CPU data
HS	=	Horizontal synchronisation
HS OUT	=	Horizontal eynchronieation output
HS SCOPE	=	Horizontal sync for digital scope board
INIT	=	Initialisation
INV	=	Invert
LDBAR	=	Load bargraph
LDSR	=	Load shift register
LVDO-LVD7	=	Latched video data
MAO-MA11	=	Memory address
MEMEN	=	Memory enable
MEMRD	=	Memory read
MEMWR	=	Memory write
OECHARGEN	=	Output enable character generator
OERAM	=	Output enable RAM (random access memory)
OPTION	=	Option
PDO-PD7	=	Pixel data
PRENBAR	=	Pre-enable bargraph

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TESTING ECRT BOARD

There are some possibilities to test the ECRT board with help of a FTU. Connect FTU to P1 of the FLOPPY DISC-RS232 INTERFACE board.
Press reset button on ECPU68K **board.**
Now you are asked to press a key on the FTU. Do this.
Now you are asked to type a password.
Type: FSE
Now you are In the monitor program.

Testing register I9 (writing a byte to it)

Type: WB218001,OO <RET>
There should be a (write) pulse on 19 pin 11 every (+/-) 200µs
All outputs of 19 should be "0"
press ESC button
Type: WB218001,FF <RET>
All outputs of 19 should be "1"
There is a (write) pulse on 19 pin 11.
(note: the display on the monitor is rubbish)
Press reset button on ECPU68K and go into the monitor program again.

Testing buffer H9 (reading a byte from it)

Type SB218001,218001,00 <RET>
Type LB218001,218001 <RET>
The monitor shows: 80 (for a 50 HZ patched board)
00 (for a 60 Hz patched board)
(50 Hz : jumper W2 out)
(60 Hz : jumper W2 in)

CRT controller (6845) test (writing / reading to / from it)

Type: WB210001,OF <RET>
There should be a repetitive pulse on pin 25 of the 6845.
press ESC button
Type: WB210003,55 <RET>
Now 55 is written into register OF of the 6845 (cursor register)
press ESC button
Type RB210003 <RET>
Now register OF is continuously read.
The monitor **must** show 55. This is what we have written to the register.
Press ESC button.

RAM test (writing and reading)
Type: WB2027FF,OO <RET>
A @ appears In lower right corner.
Check pulses on D2 pin 19 , G3 pin 27
Trigger on D2 pin 19.
During low period of D2 pin 19 the RAM (G3) pin 20 should be low.
During the low period of D2 pin 19 the RAM data lines should also be low.

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Press ESC button.
Type: WB2027FF,FF <RET>
An inverted question mark appeare in lower right corner,
During low period of D2 pin 19, the RAM data lines should be high.
Press ESC button.

Option test

Type SB202401,202401,00 <RET>
This means 00 is written to the characterO,O location.
And that means no options allowed.
A5 pin 5 must be "0"
A6 pin 9 must be "0"
Type: SB202401,202401,FF <RET,
A5 pin 5 must be "1"
A6 pin 9 must be "1"
Type: SB202401,2027FF,20 <RET>
This will clear the screen.
Type: SB202601,202601,FC <RET,
This makes a short bargraph on the left middle of the screen.
Type: SB202601,202601,80 <RET>
This makes a long bargraph under the short bargraph.

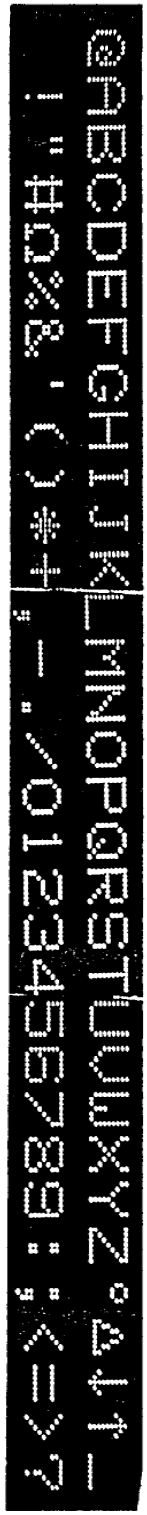
Type: SB202401,2027FF,20 <RET>
Clears the screen.
Type: SB202401,2027FF,Ol <RET>
Fills screen with "A"
Type: SB202401,2027FF,41 <RET>
Fills screen with "A" blinking.
Type: S8202401,202401,80 <RET>
Makes the "A" inverted instead of blinking.

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20 hex > < 00 hex

30 hex > < 10 hex

3F hex > < 1 hex



Character set of old CRT-controller board (7001E9311-14)

20 hex > < 00 hex

30 hex > < 10 hex

3F hex > < 1 hex



Character set of ECRT-board (7001B9311-59)
(note: 7 sets more possible)

APPENDIX A

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6845 initialisation codes

	50 HZ	60 Hz
RO	2B	2B
Rl	20	20
R2	23	23
R3	34	34
R4	13	10
R5	10	08
R6	10	10
R7	12	10
R8	00	00
R9	OE	OE
R10	00	00
Rll	OE	OE
R12	02	02
R13	00	00
R14	00	00
R15	00	00
R16	READ ONLY REGISTER (LIGHT PEN)	
R17	READ ONLY REGISTER (LIGHT PEN)	

Address 6845 registers: 21000* (hex)

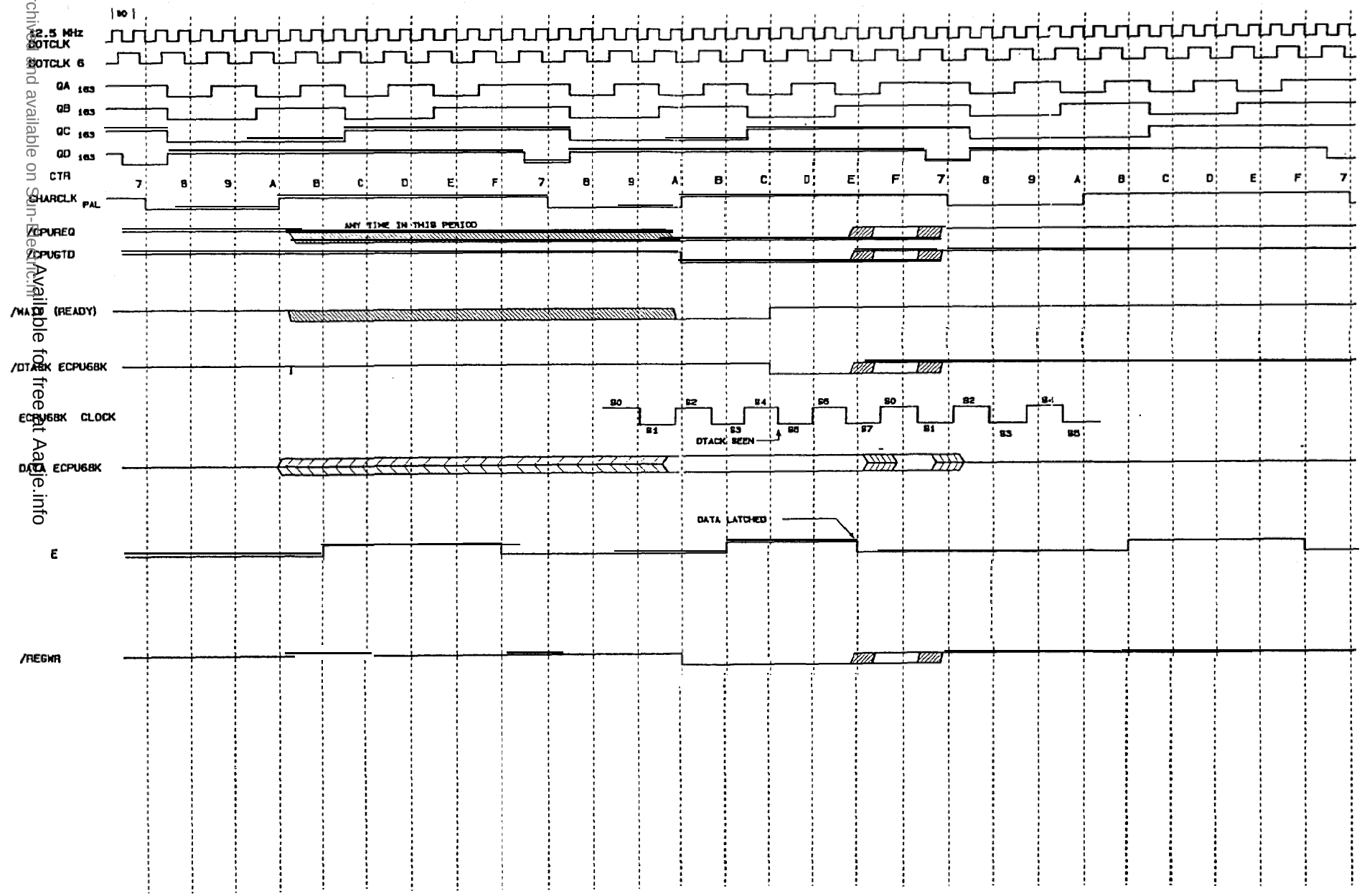
*= 1 : Byte value written to this address represents register number.

*= 3 : Byte value written to this address represents data to be loaded in the register involved.

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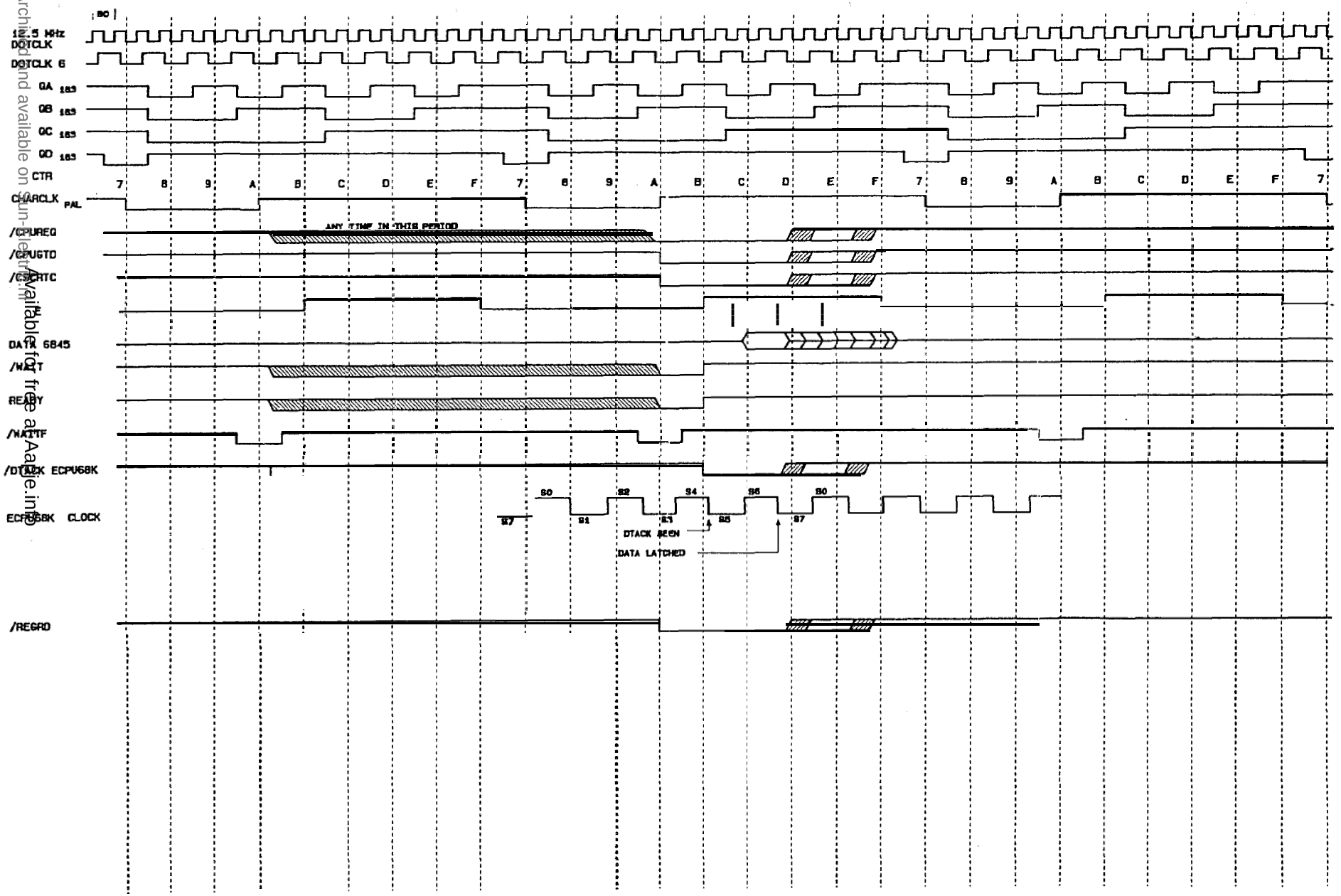
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TIMING CHART — WRITE ACTION TO 6845 AND REGISTER I9 — 0692E9306-08 — DWG. SHEET 1

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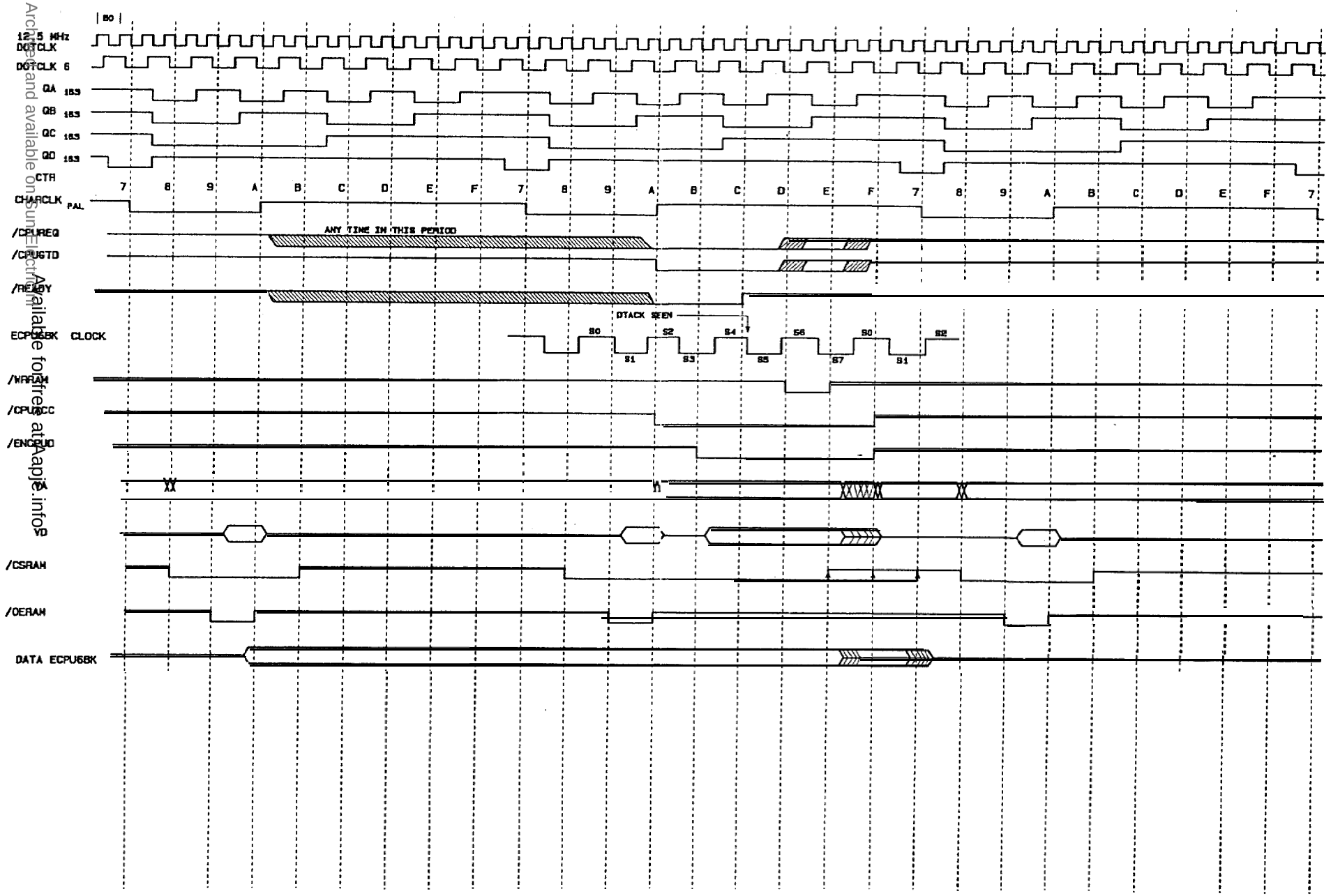
TIMING CHART

READ ACTION TO 6845 AND BUFFER H9

0692E9306-08

DWG. SHEET 2

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Available for free at Apple.info



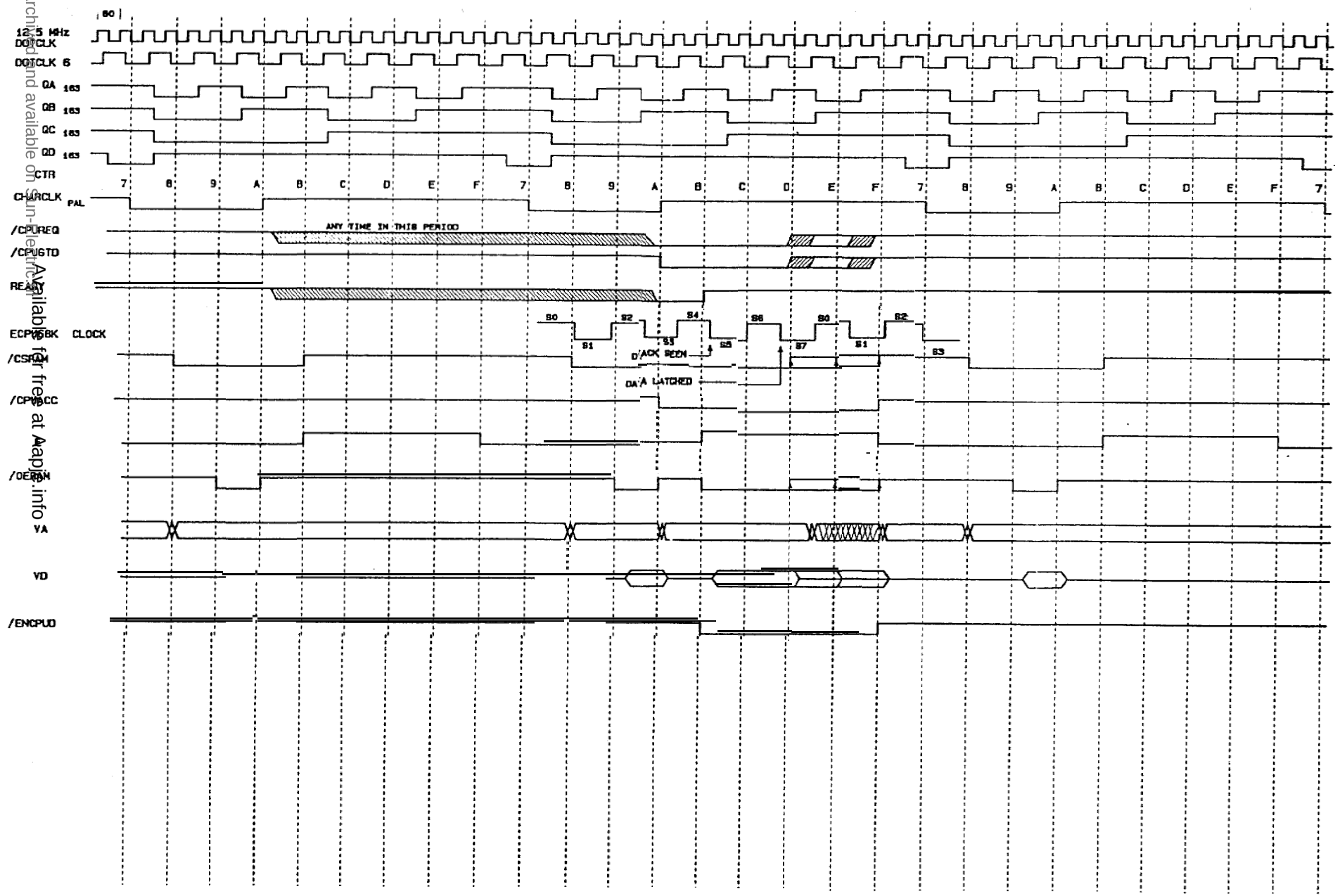
TIMING CHART

WRITE ACTION TO RAM (G3)

0692E9306-08

DWG. SHEET 3

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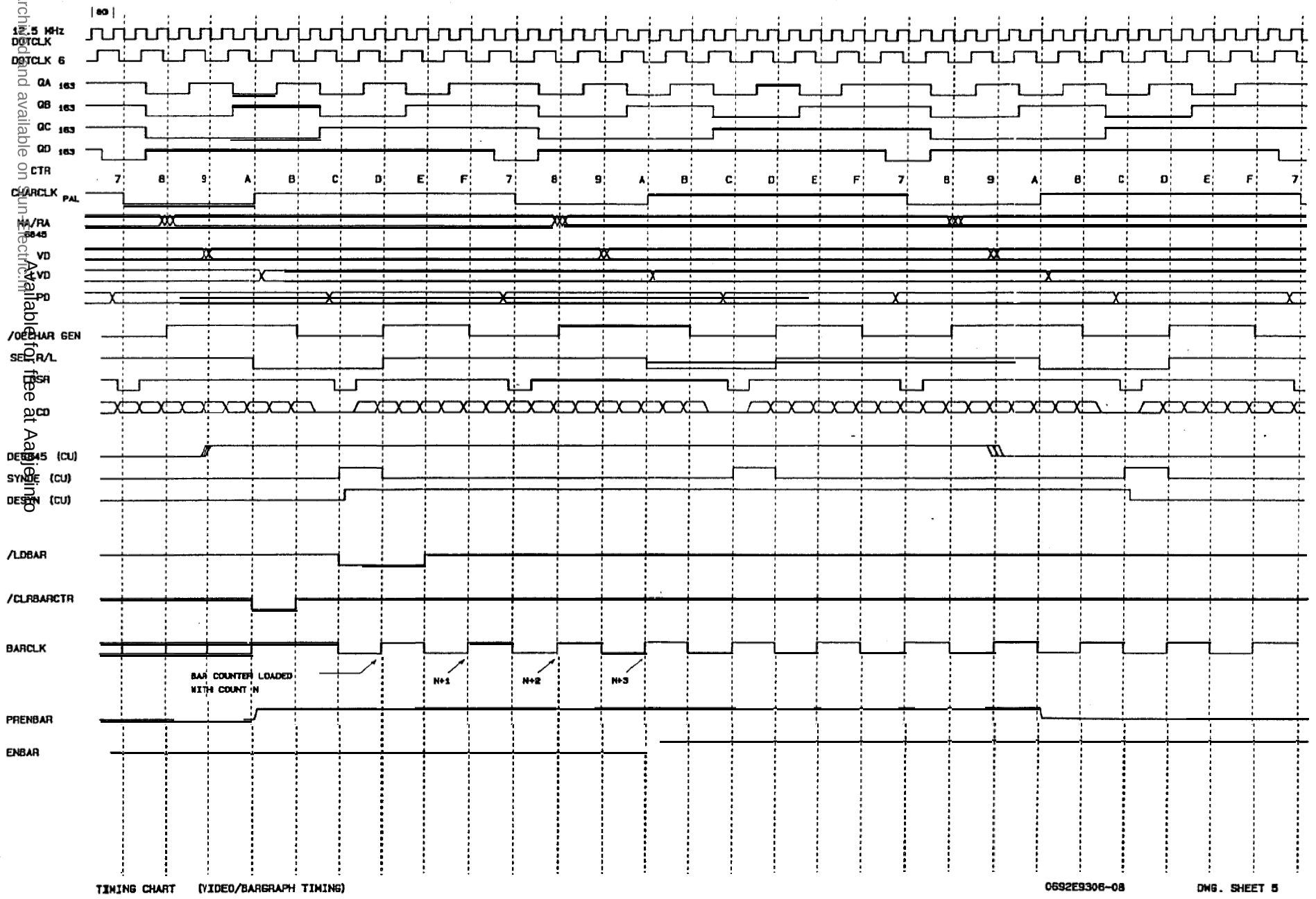
TIMING CHART

READ ACTION FROM RAM (63)

0692E9306-08

DWG. SHEET 4

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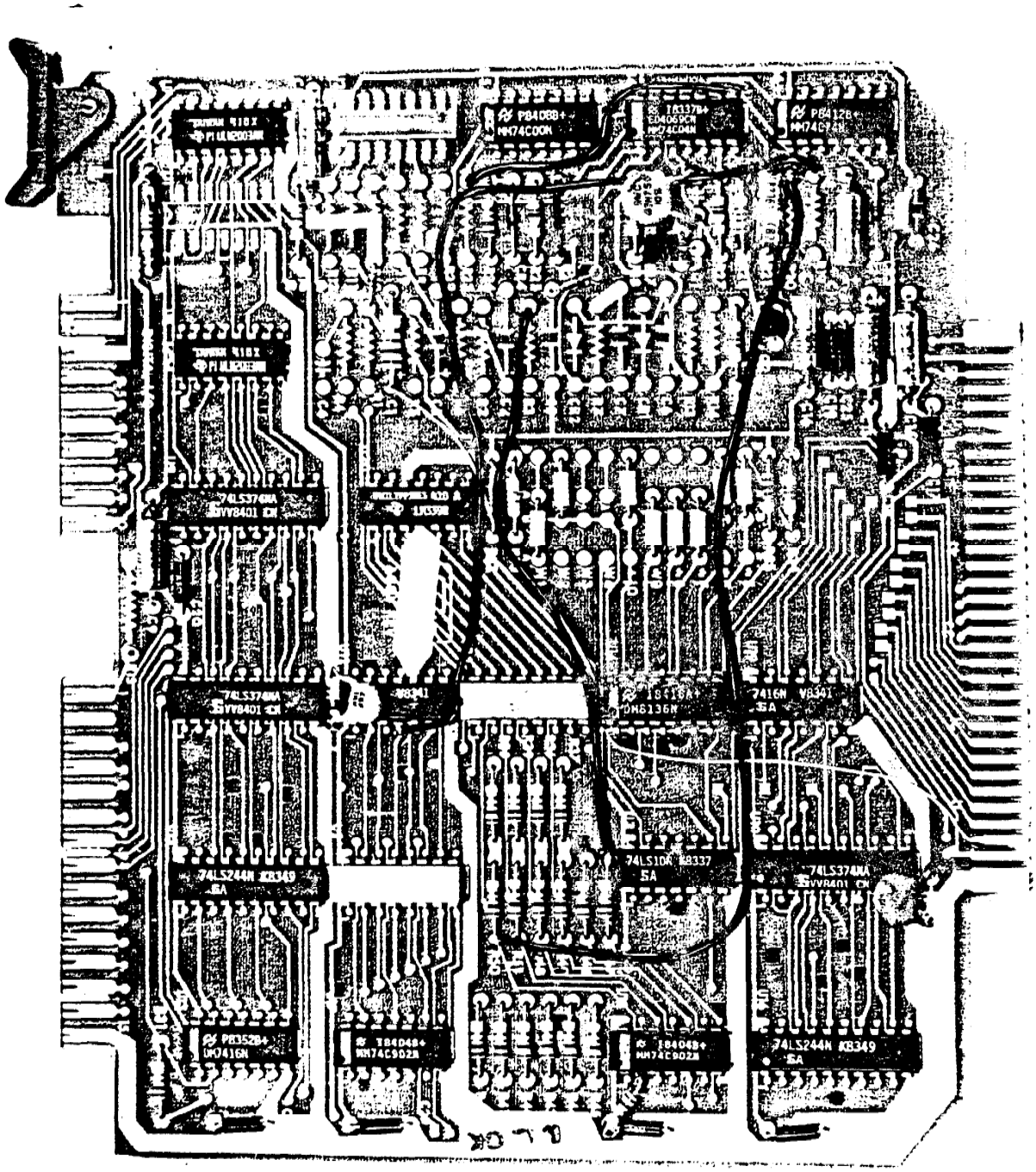


TIMING CHART (VIDEO/BARGRAPH TIMING)

0692E9306-08 DWG. SHEET 5

3.1.6

DIGITAL I/O BD.SLOT 1)



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OUTPUT CONTROLS

THE DIGITAL I/O ALLOWS THE COMPUTER TO EXECUTE THE FOLLOWING CONTROLS OVER THE ANALOG SECTION OF THE TESTER.

P206 PIN No	SIGNAL	USE	DESTINATION
J	$\overline{\text{ENG KILL}}$	THIS SIGNAL IS ACTIVATED AUTOMATICALLY BY THE COMPUTER DURING CRANKING TESTS OR MANUALLY VIA THE REMOTE CONTROL (ACTIVATE "A" SENSE "4"). ENGINE KILL IS USED BY THE MISC FUNC BOARD TO PRODUCE SHORT (SEE SECTION 4)	MISC FUNC PIN 17 SEE SECTION 4
6	$\overline{\text{VOLTS}}$	THIS SIGNAL IS ACTIVATED VIA THE REMOTE CONTROL CURSOR BUTTON(ACTIVATED SENSE 8) WHILST IN THE SECOND MULTI-METER PAGE (SEE FLOW DIA. INTRODUCTION.) VOLTS IS USED BY THE VOLT/OHM BD TO SWITCH BETWEEN VOLTS AND OHMS. NOTE: THE COMPUTER WILL HOLD THE VOLT LINE Low (VOLT/AMP BD IN VOLTS MODE).	VOLT/OHM PIN J SEE SECTION 4

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OUTPUT CONTROLS (CONT.)

P206 PIN No	SIGNAL	USE	DESTINATION
6 (CONT.)	VOLTS	SHOULD A VOLTAGE BE DETECTED AT THE PROBES. INHIBITING THE OPERATOR FROM SELECTING THE OHMS RANGE. DUE TO STRAY PICKUP IT MAY BE NECESSARY TO SHORT THE LEADS BEFORE SELECTING OHMS.	
F	OHMS X 1K	THIS SIGNAL IS ACTIVATED AUTOMATICALLY BY THE COMPUTER. OHMS X 1K IS USED BY THE VOLT/OHM BD TO SWITCH THE OHM RANGE BY A FACTOR OF 1000 WHEN IN THE OHMS MODE.	VOLT/OHM PIN D SEE SECTION 4
9	CPU CAL	NOT USED: SEE SOFTWARE UPDATES AND OPTIONS SECTION 11	VOLT/OHM PIN N
7	100 A	THIS SIGNAL IS ACTIVATED AUTOMATICALLY BY THE COMPUTER. 100 A IS USED BY THE AMP/TEMP BD TO SWITCH TO THE 100 A RANGE DURING CALIBRATION AND CCNNECTION CHECKS	AMP/TEMP PINS B AND S

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OUTPUT CONTROLS (CONT.)

P206 PIN No	SIGNAL	USE	DESTINATION
H	$\overline{\text{FORCE STROBE}}$	THIS SIGNAL IS ACTIVATED AUTOMATICALLY BY THE COMPUTER DURING CRANKING MEASUREMENTS. $\overline{\text{FORCE STROBE}}$ IS USED BY THE TIMING BD TO SELECT STROBE TIMING ALTHOUGH MAG TIMING IS AVAILABLE.	TIMING BD PIN 3 SEE SECTION 4
4	$\overline{\text{PURGE}}$	THIS SIGNAL IS ACTIVATED AUTOMATICALLY BY THE COMPUTER DURING CALIBRATION. $\overline{\text{PURGE}}$ IS USED BY THE IR INTERFACE TO SWITCH ON THE PURGE SOLENOID AND OVERRIDES THE $\overline{\text{PUMP}}$ ON SIGNAL FROM THE FRONT PANEL	IR INTERFACE J1 PIN 2 SEE SECTION 7
E	$\overline{\text{SPAN}}$	THIS SIGNAL IS ACTIVATED AUTOMATICALLY BY THE COMPUTER DURING CALIBRATION. $\overline{\text{SPAN}}$ IS USED BY THE IR INTERFACE TO SET THE ELECTRONIC SPAN RELAY ON THE GAS PROCESSING BD.	IR INTERFACE J1 PIN 3 SEE SECTION 7

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TESTER STATUS

P205 PIN NO	SIGNAL	USE	SOURCE
6	TL HOLD	FREEZES DISPLAYED TIMING READINGS DURING STROBOSCOPIC MODE.	TIMING LIGHT
5	EURO MAG	NOT USED. SEE SOFTWARE UPDATES AND OPTIONS SECTION 11	TIMING BD
	0^0 SYS FIL	NOT USED. SEE SOFTWARE UPDATES AND OPTIONS SECTION 11	TIMING BD
8	CYL # 1	NOT USED. SEE SOFTWARE UPDATES AND OPTIONS SECTION 11	PRE-PROCESSOR

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DIGITAL I/O

THE DIGITAL I/O BOARD SLOT 1 HAS HAD ONE EXTRA OUTPUT FUNCTION ADDED:

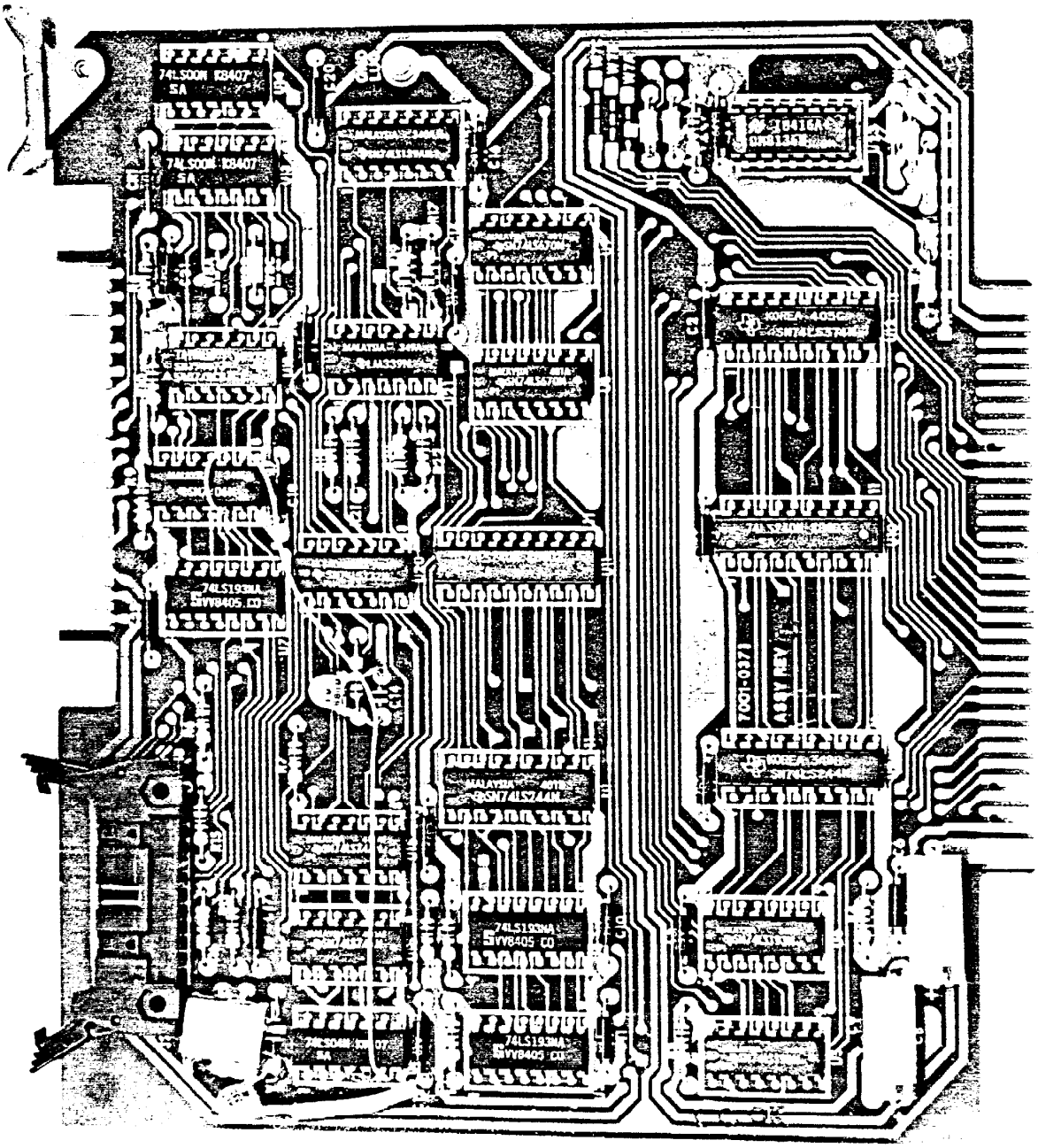
THIS IS :

P206	SIGNAL	USE	DESTINATION
PIN 5	DIESEL SELECT	THIS SIGNAL IS ACTIVE IF A DIESEL CAR HAS BEEN SELECTED IN THE VEHICLE SELECTION PAGE.	SEE SECTION 5.3 DIESEL OPTION

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3.1.7

KV CARDREADER BD.(SLOT 2)



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F. K.V. CARDREADER BD.(SLOT 2)

THE K.V. CARDREADER HAS TWO USES WITHIN THE TESTER:

1. TO CONTROL THE K.V. PROCESSOR AND K.V. SLOPE BDS IN THE ANALOG RACK.
2. TO ACT AS AN INPUT FOR THE GAS BENCH IDENTIFICATION LINES.

1. THE K.V. CARD READER IS CONTROLLED BY THE CPU VIA THE BACKPLANE BUSSES AND PRODUCES THE FOLLOWING OUTPUTS:

OUTPUT	J1 EDGE CONNECTOR PIN
RIPPLE CHK	9
/TEST	7
± PEAK SELECT	M
$\overline{\text{READ}}$	K
DISCHARGE	8

THESE OUTPUTS CONTROL THE MEASUREMENT PROCESSES AND AUTO CALIBRATION CARRIED OUT ON THE K.V. PROCESSOR AND K.V. SLOPE BDS (SEE SECTION 4).
THE SEQUENCE AND TIMING OF THESE SIGNALS IS DICTATED BY THE SOFTWARE CONTAINED ON THE PROGRAM MEMORY BD.
A SIGNAL RING CNT (J1 PIN J) IS INPUTTED TO THE. K.V. CARD READER. THIS SIGNAL IS GENERATED BY THE K.V. PROCESSOR TO INFORM THE COMPUTER THAT THE SPARK DURATION IS COMPLETE AND READY FOR READING AND DISPLAY.

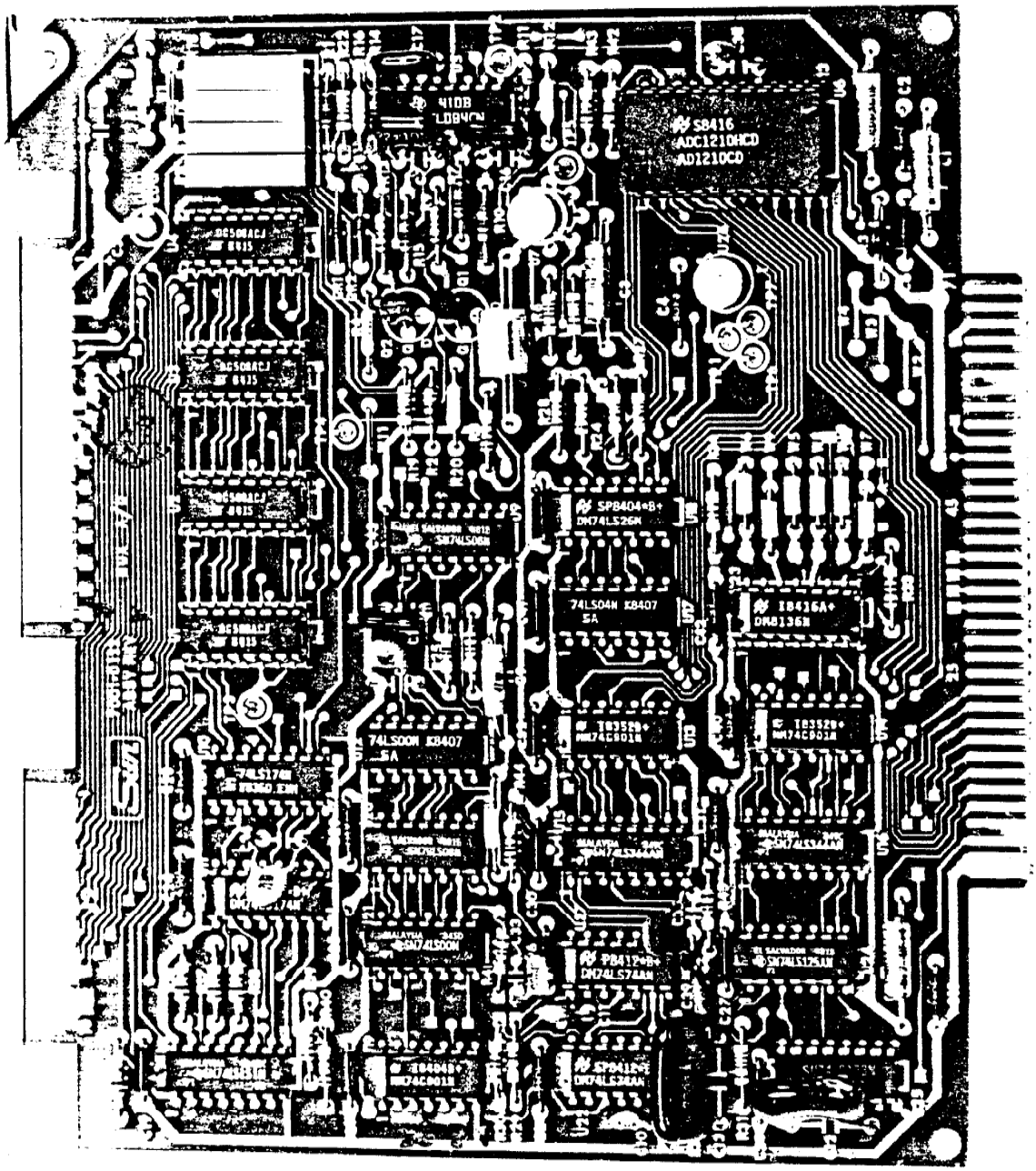
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2. THE K.V. CARD READER ACTS AS AN INTERFACE TO ALLOW THE CPU TO SCAN THE GAS BENCH IDENT LINES CONNECTED VIA THE 20 PIN RIBBON CONNECTOR. THESE LINES ALLOW THE COMPUTER TO DETERMINE IF A GAS BENCH IS FITTED AND WHAT GASSES ARE AVAILABLE. THE LOW FLOW SIGNAL IS ALSO SCANNED AT THIS POINT (SEE SECTION 7).

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3.1.8

MUX A/D BD. (SLOT 3)



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C. MUX A/D BOARD (SLOT 3).

MANY OF THE PARAMETERS MEASURED BY THE MCS-2000 ARE DETERMINED BY ANALOG MEANS. SINCE ALL PARAMETERS ARE DISPLAYED DIGITALLY, THE ANALOG VOLTAGES MUST BE CONVERTED INTO DIGITAL FORM.

A SINGLE A/D CONVERTER IS USED TO CONVERT ALL THE ANALOG CHANNELS, ONE AT A TIME. THE SWITCHING OF THE A/D BETWEEN CHANNELS IS ACCOMPLISHED BY A MULTIPLEXER (MUX). THE MUX A/D INPUT RANGE ON ALL CHANNELS IS LIMITED TO ± 7V, THE SOFTWARE THEN TAKES THE RESULTANT DIGITAL OUTPUT AND CONVERTS IT INTO THE DISPLAYED READINGS. THE CONVERSION FACTOR VARIES ACCORDING TO THE CHANNEL.

AS WELL AS CONVERTING THE DIGITAL SIGNALS THE SOFTWARE MONITORS SOME INPUTS TO DETERMINE EITHER CALIBRATION LIMITS OR CONNECTION CHECKS.

THE FOLLOWING TABLE LISTS THE ANALOG CHANNELS THAT ENTER THE MUX A/D THERE CONVERSION FACTORS AND WHERE APPLICABLE THERE CONNECTION AND OR CALIBRATION VOLTAGES.

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* NOT APPLICABLE

CONNECTOR	PIN	TESTER FUNCTION	CONNECTION VOLTAGE	CALIBRATION VOLTAGE	SOFTWARE CONVERSION FACTOR
P902 J2	K	GROUND	*	*	1
P902 J2	D	HC ANALOG	*	± 1.25 v	SEE GRAPH PAGE 8
P902 J2	E	CO ANALOG	*	± 1.25 v	SEE GRAPH PAGE 9
P902 J2	4	CO2 ANALOG	*	± 1.25 v	SEE GRAPH PAGE 10
P902 J2	A	SPK KV2 ANALOG	*	*	7V = 8 KV
P902 J2	J	SPK KV1 ANALOG(NOT USED)	*	*	*
P902 J2	B	PK KV ANALOG	*	1	7V = 49 KV
P902 J2	C	RIPPLE VOLT ANALOG	*	*	2.87V = 10.2% @ 13V BATT
P902 J2	F	SECONDARY AVAILABLE	> 4v	*	*

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* NOT APPLICABLE

CONNECTOR	PIN	TESTER FUNCTION	CONNECTION VOLTAGE	CALIBRATION VOLTAGE	SOFTWARE CONVERSION FACTOR
P902 J2	H	KLI5 (COIL +) ANALOG	> 4.5v	*	7v = 15v
P903 J1	2	GND ANALOG	*	*	*
P903 J1	N	KL1 ANALOG	*	*	7v = 15v
P903 JI	K	BATTERY ANALOG	> 4 V	*	7v = 40.5v
P903 J1	11	TEMP ANALOG	*	> 6.9v	1.4v Ω 100°C
P903 J1	I2	VAC ANALOG	*	+3 TO 7v	SEE GRAPH PAGE 11
P903 J1	8	AVE AMP ANALOG	> ± 70mV	± 2.ov	7V= 1000A
P903 JI	M	RAW AMP ANALOG	*	*	7V = 1000A
P903 J1	13	V/ ANALOG	SHORT -5 TO -7V * OPEN +5 TO +7V		7v = 40v
P903 J1	6	PRIMARY AVAILABLE	>4v	*	*

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THE FOLLOWING SIGNALS ARE NOT MULTIPLEXED INTO THE A/D.

P903 (J1)

PIN

R ---------- DELAYED DWELL

THIS SIGNAL IS USED
BY THE MUX A/D
BOARD TO DETERMINE
WHEN THE POINTS ARE
CLOSED FOR DYNAMIC
KL1 AND
KL15 READINGS

15 ---------- CYL CLK

THIS SIGNAL IS USED
BY THE MUX A/D
BOARD TO DETERMINE
WHEN EACH CYLINDER
IS AT MAXIMUM COM-
PRESSION FOR AMPS
PER CYLINDER
READINGS (RAW AMPS)

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P902 (J2)

PIN

L ---------- GAS BENCH GND.

THIS LINE (IF CONNECTED) TELLS THE MUX TO SCAN THE GAS ANALOG INPUTS

ALL FUNCTIONS OF THE MUX A/D BOARD ARE UNDER THE DIRECT CONTROL OF THE CPU BOARD VIA THE BACKPLANE BUSSES.

BEFORE AN A/D CONVERSION CAN TAKE PLACE THE CPU MUST SEND SEVERAL PIECES OF INFORMATION TO THE MUX A/D BOARD VIA THE BACKPLANE BOARD.

THESE ARE:

1. CHANNEL — TELLS THE MUX WHICH SIGNAL IS TO BE APPLIED TO THE A/D CONVERTER.

2. GAIN — SETS GAIN (PRIOR TO A/D CONVERSION) TO ONE OF TWO RANGES. THE LOW RANGE IS USED TO INCREASE RESOLUTION ON LOW LEVEL SIGNALS.

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3. TRIGGER MODE — DETERMINES "HOW" THE START OF CONVERSION IS TO BE MADE. IN THE EXTERNAL MODE, THE CPU BOARD ISSUES THE START CONVERSION COMMAND. IN THE INTERNAL MODE THE START CONVERSION COMMAND IS GENERATED ON THE MUX A/D BOARD. TO COINCIDE WITH A CHOSEN EVENT, SUCH AS POINT CLOSE, (USED DURING KL1 AND KL15 VOLTAGES) OR CYL CLOCK (USED FOR AMPS/CYLINDER).

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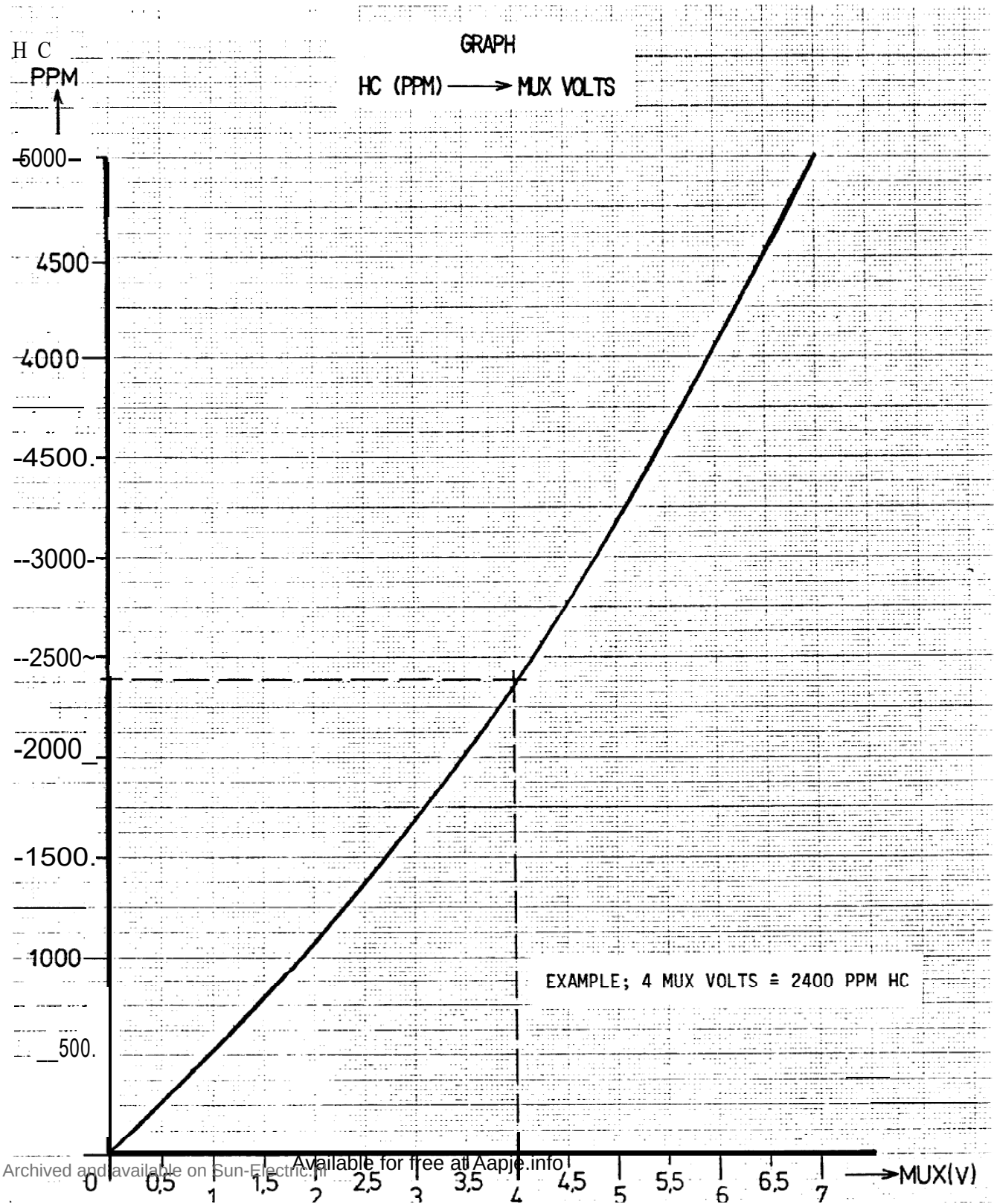
4. START CONVERSION — IN THE EXTERNAL MODE. THE CPU ISSUES THE START CONVERSION COMMAND.

WHEN THE MUX A/D BOARD HAS MADE THE REQUESTED CONVERSION, IT SIGNALS THE CPU BOARD VIA THE BACKPLANE BUSSES. THE CPU THEN READS IN THE CONVERTED DATA AS A 12 BIT BINARY NUMBER VIA THE BACKPLANE BUS. THE CPU BOARD CONVERTS THIS BINARY NUMBER INTO A FORM SUITABLE FOR DISPLAY.

THERE ARE FOUR POTENTIOMETERS SITUATED ON THE MUX A/D BOARD THAT ALLOW FOR THE ADJUSTMENT OF THE SAMPLE AND HOLD RATE AND THE REFERENCE VOLTAGES. THESE POTS ARE FACTORY SET, AND SHOULD NOT BE ADJUSTED BY THE FIELD SERVICE ENGINEER.

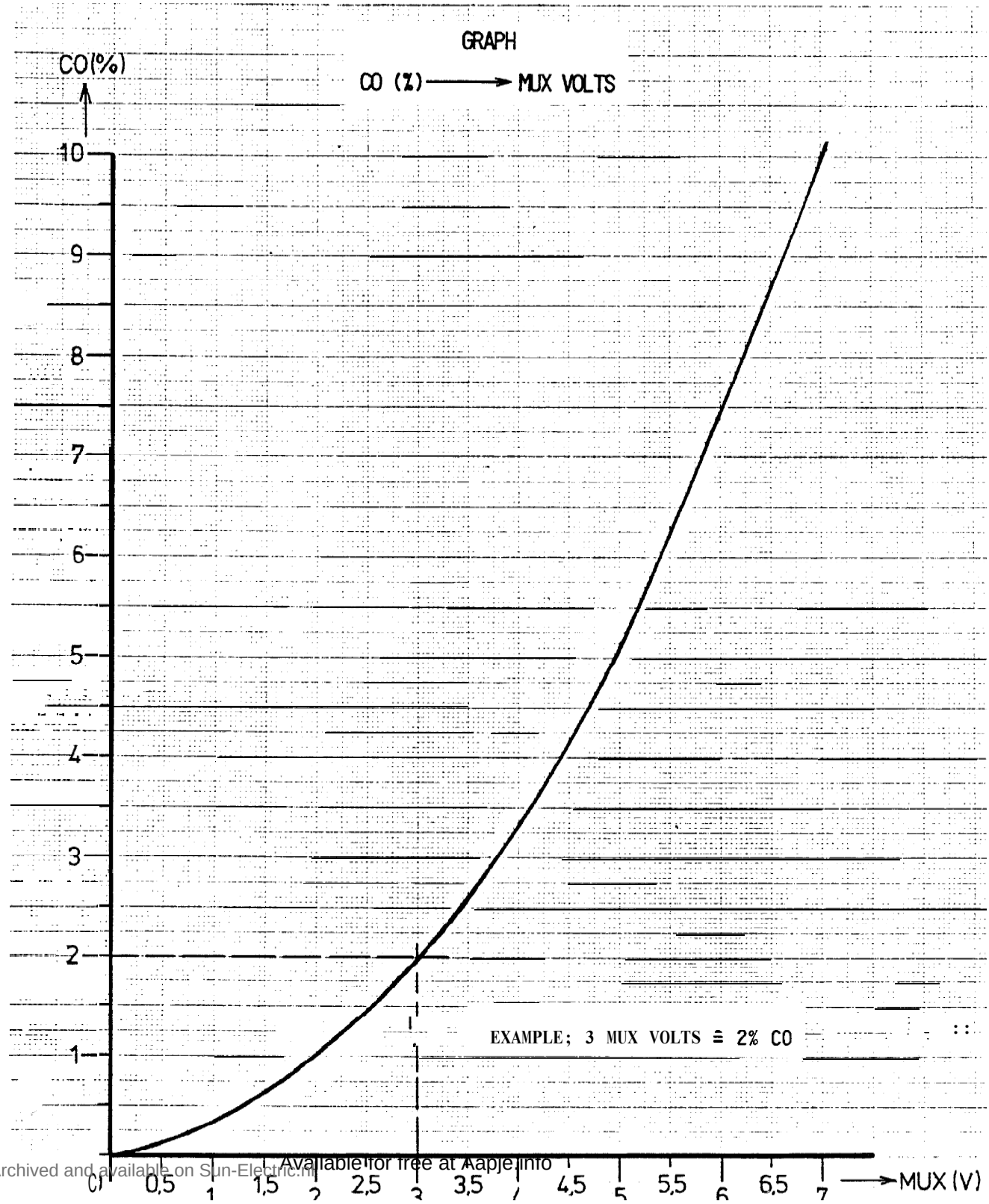
THE MUX A/D BOARD IS CRITICAL IN ALL ASPECTS OF CALIBRATION CONCERNING THE SUN-2014 AND THEREFORE A FULL CALIBRATION PROCEDURE MUST BE CARRIED OUT IF IT IS CHANGED IN THE FIELD. SEE SECTION 1

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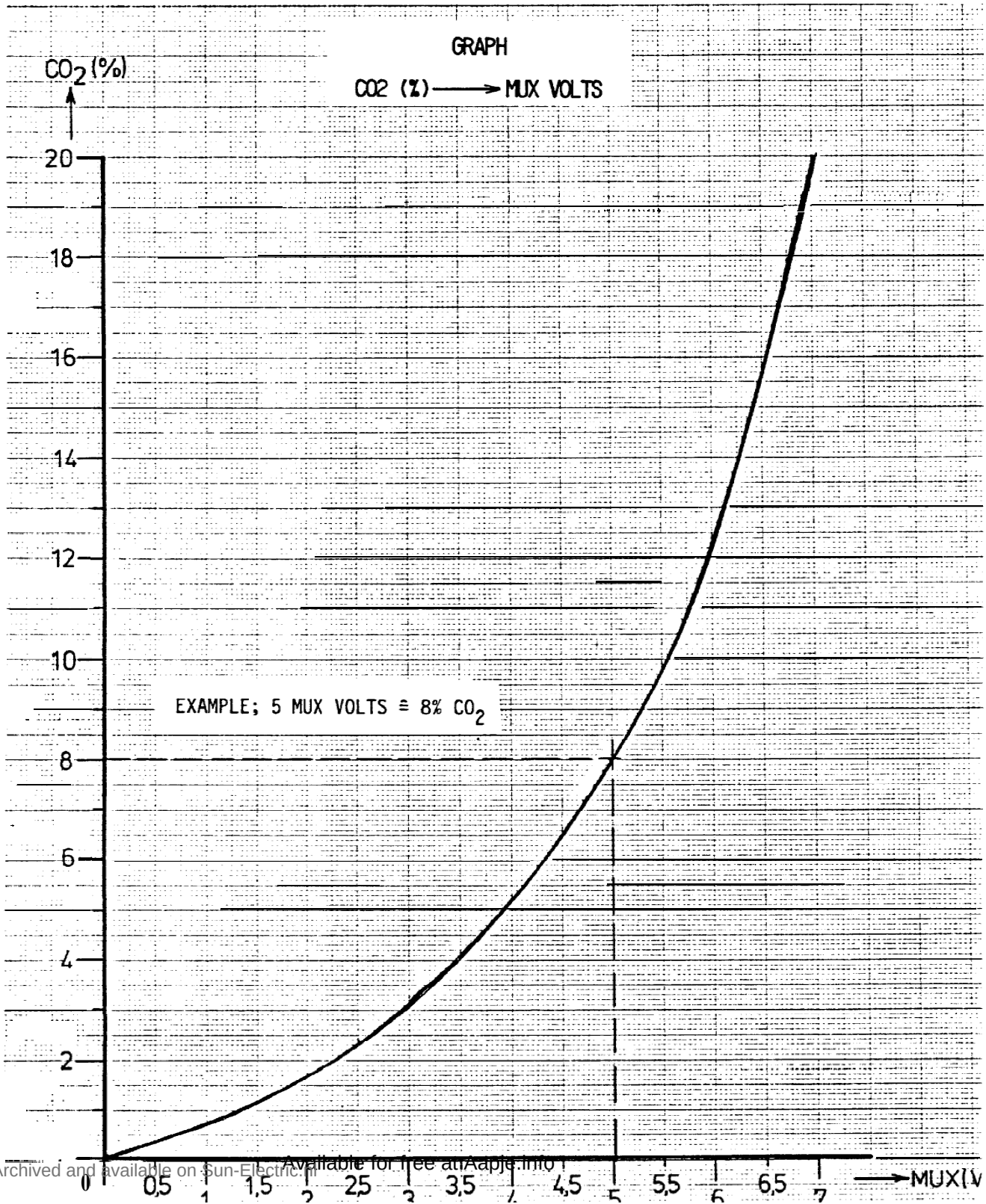
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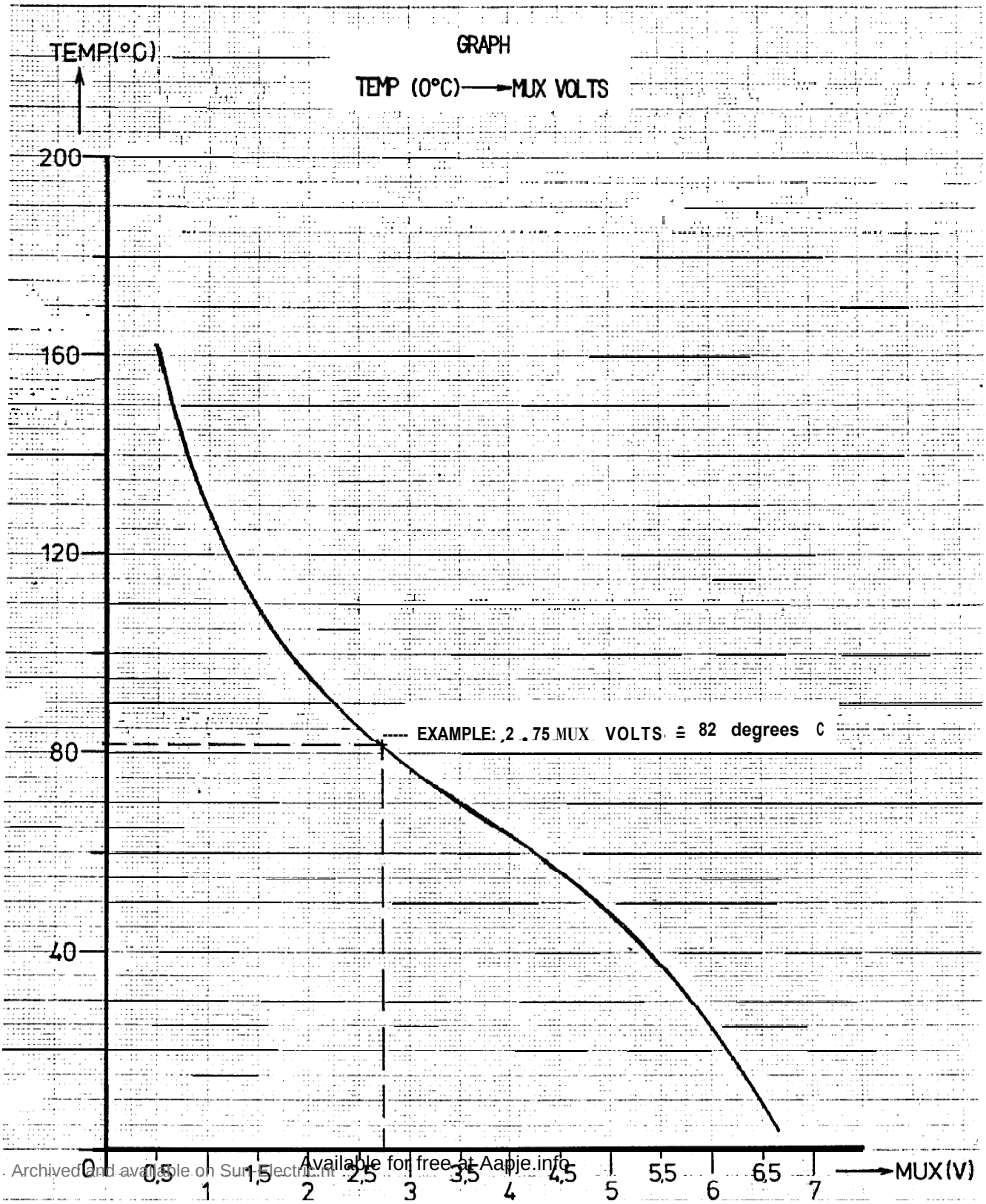
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FUNCTIONAL DESCRIPTION

MUX ADC BOARD 7001E9313-27

MCS/OCS - 2000

PART NUMBER: 0692E9310-24

From : SEE Engineering - K. Stam

Approved : B. Gee Date: 31. 3.94

Checked : Peter Tel Date: 31. 3.94

Date : MARCH 1994
ERN : 1124
ECN : --
Rev. : A
Ref.nr. : PC

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1. GENERAL

The MUX ADC board converts the supplied analog signals into a digitised value. It contains 32 input channels of which 3 channels are reserved to get the zero and span voltages. The board converts analog signals up to +/-7.35V into a 12-bit word. The board is controlled by the ECPU68K board (7001E9311-44) or the older CPU/RAM board (7001E9004). From here a channel selection and a trigger selection can be made. A trigger selection is used to start a conversion at a predefined time. After conversion the digital value is available on the bus and an interrupt is generated. When the data is being read a new conversion could be started

The reason for replacing the older MUX A/D board 7001E9012 is that the applied ADC is getting obsolete. The new board (7001E9313-27) is fully interchangeable with the older board so this board can also be used in the OCS/MCS2000, SAM4000 and SUN2014 testers.

For detailed information refer to:

- Schematic MUX ADC 7092E9313-27
- Assy MUX ADC 7001E9313-27
- PCB MUX ADC 7025E9313-27

SPECIFICATIONS

SUPPLY

+12V	60 mA (15 mA)
-12V	25 mA (5 mA)
+5v	100 mA (100 mA)

Note.that the supply voltages are also used for the supply of the gas measuring module. Between the brackets the values are given without connection of the gasbench.

ACCURACY

resolution 3.66 mV (x1 amplification)
resolution 0.916 mV (x4 amplification)

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2. FUNCTIONAL DESCRIPTION

The MUX ADC board contains multiplexers (U10 and U11) which provides 32 input channels. When an input channel is selected the trigger enable must be disabled to avoid that a conversion is started. (Bit D15 is 'HIGH' and bit D12- is 'LOW). The outputs of the multiplexers are buffered, amplified (U12), filtered and connected to the A/D converter. (U13). The amplification of U12 can be switched X1 (Bit D5 = 'LOW = amplify 1 times) or X4 (Bit D5 = 'HIGH' = amplify 4 times)
(Note that selection and amplifying only takes place when bit D7 is high.)

The trigger gal (U8) provides a trigger signal which, together with the monostable multivibrator (U9), generates a trigger pulse of 1 µs to start the conversion. The data bits, which are latched, select 1 of 8 trigger signals. (See document 0733E057*-64 for the formulae)

A trigger selection consists of two writes at the specified address range. In this selection also a choice has to be made whether an interrupt has to be made after conversion or not. The first write selects a trigger input when the trigger enable is 'LOW, so that a change in signal level at the output, caused by the different signal input levels, will be disabled. It is also possible to combine the Input channel sel. write and the first Trigger sel write. The second write contains the same data but the trigger enable is 'HIGH' now.

(Note that selection only takes place when bit D15 is high).

Trigger input 1 and 8 are internal trigger inputs and can be manipulated by software. Input 1 will directly give a trigger when the trigger enable is 'HIGH'. A trigger will be generated only when a rising edge is detected. When Trigger input 8 is selected, the output will give a trigger when a write to the adress range with the data 0800H (Bit 11). After conversion and the converted data is read, another trigger could be generated.

A minimum of 2 writes are needed to start the conversion. The first write is to select an analog input channel and the trigger channel. After ±80 µs a second write enables the trigger signal (trigger enable).

The standard input range for the MUX ADC board on all channels:

-7.35 to 7.35 Volt for 1 time amplification
-1.8375 to 1.8375 Volt for 4 times amplification

This range is converted with 12 bits. This means that the resolution is:

(10 - (-10)) / (212xl -33) = 3.66 mV (xl amplification)
(10 - (-10)) / (212x5.33) = 0.916 mV (x4 amplification)

The conversion will be triggered by the first falling edge of the selected trigger signal. During the conversion the signal /CC is 'HIGH' to indicate that the converted data is not available. A write will not disturb the conversion during the conversion cycle.

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After a conversion is completed the data can be accessed by a read action to the buffers U1 and U2, at the specified adress range to obtain a word. D15 contains the MSB and D4 the LSB of the converted analog signal. The bits D4 to D15 are represented in two's complement. The bits D1 to D3 are used for board recognition. When the conversion is done succesfully, bit DO is set to 'HIGH'. This bit will be reset after a write to the specified address range.

The adjustment procedure has to be done by software. Input channel 1 contains the offset voltage. input channel 2 and 3 contains respectively the voltage 7.35V and 1.8375. These voltages are derived from the reference voltages of the ADC. After a conversion and the data is valid (bit D0 = 1), the counts has to be shifted to the right 4 times, noting that the MSB will be shifted in. (This is done in the current software)

The counts of any input channel wiil be:

Amplification = 1

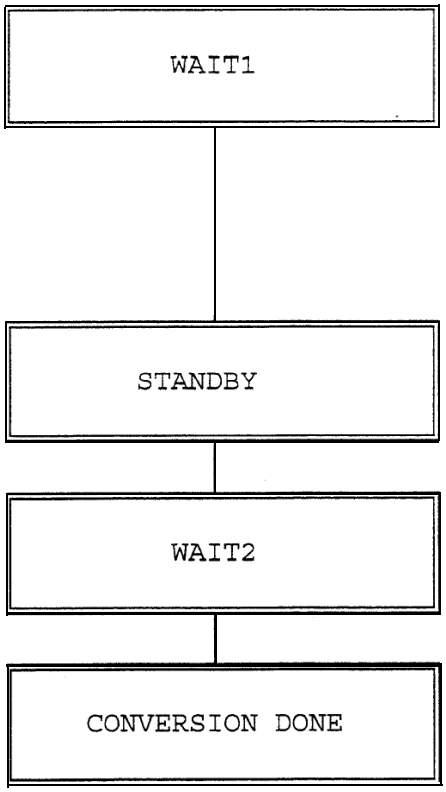
$$\text{inp channel} = \frac{\text{any inp. channel} - \text{input channel 1}}{\text{input channel 2} - \text{input channel 1}} * 7.35\text{v}$$

Amplification = 4

$$\text{inp channel} = \frac{\text{any inp. channel} - \text{input channel 1}}{\text{input channel 3} - \text{input channel 1}} * 1.8375\text{V}$$

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Summary the conversion cycle can be divided in 4 conditions which are given below:



At this condition a new trigger and mux. channel will be selected when D7 and D15 are active. The int. and bit D0 will always be disabled. After the write condition STANDBY will be active. Only when Bit Dll (data= 0800h)is active condition WAIT2 will be active

At this condition the conversion could be started by the sec. trigger write.

At this condition the gal (U7) will wait until the conversion is completed.

At this condition the interrupt will be activated The data at the output can be read. A write activates condition WAITl.

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3. FUNCTIONAL REFERENCE SIGNALS

All the input and output signals from and to the data, address and control bus are buffered with U1, U2, U3, U4 and U5 to increase the noise immunity and the driving capability.

The MUX ADC board is selected when address range 800140h - **80015Fh** is activated. With the additional data the following I/O functions can be performed;

	WRITE		READ	
D15	**ENABLE WRTRIG**	**(DI15)**	D B 1 1	(DO1 5)
D14	*	(DI14)	DB10	(DO14)
D13	*	(DI13)	DB9	(DO13)
D12	TEN	(DI12)	D B 8	(DO12)
D11	SOFTTRIG	(DI11)	D B 7	(DO11)
D10	T S E L 2	(DI10)	D B 6	(DO10)
D9	TSEL1	**(DI9)**	DB5	(DO9)
D8	TSELO	(DI8)	DB4	(DO8)
D7	ENABLE WRMUX	(DI7)	DB3	(DO7)
D6	IEN	(DI6)	DB2	(DO6)
D5	x4/x1	(DI5	DB1	(DO5)
D4	MSEL2	(DI4)	DBO	(DO4)
D3	MSEL1	(D13)	BREG2	(DO3)
D2	MSELO	(DI2)	BREG1	(DO2)
D1	MUXSELECT	(DI1)	BREGO	(DO1)
D 0	CHANHIGH	(DI0)	C D O N E	(DO0)

where: DO through D15 are the data bits.
DIO through DI15 are the buffered input bits
DO0 through DO15 are the buffered output bits

ENABLE WRTRIG	enables a write to the latches of the trigger gal (U8), TEN and IEN
TEN	enables the trigger output of U8
SOFTTRIG	generates a software trigger
TSELO-TSEL2	are output bits to make a selection of 8 trigger channels
ENABLE WRMUX	enables a write to the latches of MUX's (U10,U11) and x4/x1.
IEN	is an output control signal to generate an interrupt after conversion.
x4/x1	is an output control signal to get an amplification of 4 times
MSELO-MSEL2	are output bits to make a selection of 8 multiplexer channels

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MUXSELECT	is an output control signal to select the other MUX (U11)
CHANHIGH	is an output control signal to select channels 9 to 16 of the selected multiplexer
BDO-BD11	are the data bits of the converted analog signal.
BREG0-BREG2	are the data bits used for board recognition.
CDONE	is a control signal to indicate that BDO-BDI 1 are valid.

4. JUMPER SETTINGS

Boardrecognize	(default setting)	W1 =A
If a minimum conversion time of 95 µsec is required: Used when the MUX ADC board is a replacement of the older board (7001E9012)		W2=A

5. ADDITIONAL CONFIGURATION POSSIBILITIES

Standard no adjustment is needed so the fixed resistors R27 and R28 are installed. The gain and offset errors are equal to the specifications of the ADC. When the gain and offset errors must be adjusted to zero, the two potentiometers RV27 and RV28 must be installed, R27 and R28 must be removed.

Standard the circuitry with R22 is used for buffering the reference voltage of the ADC. When the reference voltage is not 10V or a higher outputvoltage is needed, a non inverting amplifier can be implemented with R22 and R23.

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6. SIGNAL DESCRIPTION

BA5 - BA10	Address lines from address bus (generated on CPU).
BDO - BD15	Data lines from/to data bus.
IORD	INPUT/OUTPUT -READ. Active when processor reads from IO device.
IOWR	INPUT/OUTPUT WRITE Active when writes to IO device.
CLK4M	Clock signal from CPU (4MHz).
A5 -A10	'on board' address lines. Buffered BA5 - BA10 signals.
DI0 - DI15	'on board data input lines. Buffered BDO - BD15 signals.
DO0 - DO15	'on board data output lines. Buffered BDO - BD15 signals.
/INIT	Initialize. Initializes the MUX ADC board on a power on or reset-cycle.
/IRD	'on board' read signal. Active when address range 800140h - 80015Fh is selected and IORD is active. Enables/disables buffers U1 and U2.
/WR	'on board' write signal. Active when address range 800140h - 80015Fh is selected and IOWR is active.
/WRT	Inverted /RD signal. Enables/disables buffers U3 and U4.
CDONE	Conversion done signal. Active when /CC becomes active after a /SC.
/SC	Start conversion. Starts the conversion cycle of the ADC.
MCTIME	MINIMUM CONVERSION TIME. The minimum time required before reading the data. Constantly activated when jumper W2 is placed at point B.
/INT2,3,4,5	INTERRUPT. This output to the CPU board indicates an end of A/D conversion. It results in an INTERRUPT request to the 68000.
/IEN	INTERRUPT ENABLE. This signal is latched with D16 after a /WRTRIG.

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TRIGSTART	TRIGGER STARTS the conversion when the decoder is in the condition STANDBY.
/WRMUX	WRITE MUX signal. (/WR is gated with Bit DI7) Bits DI0, DI1, DI2, DI3, D14 and DI5 are latched when active.
/WRTRIG	WRITE TRIGGER signal. (/WR is gated with bit DI15) Bits DI6, DI8, DI9, DI10 and DI12 are latched when active.
x4/x 1	AMPLIFICATION 4x. Amplification is 4x when active, otherwise 1x. Signal is latched with DI5 after a /WRTRIG.
SOFTTRIG	TRIGGER GENERATED BY SOFTWARE. (Bit DI11 is gated with /WR).
CHANNEL 1-32	Analog inputs. range depending of amplification. 1x -7.35 to +7.35 volt. 4x -1.8375 to 1.8375 volt. input impedance > 1 Mohm.
/DELAYED DWELL, CYL CLOCK	TRIGGER INPUTS. input signals 0V/12V. Active at the rising edge of the signal.
TRIGGER 4 - 7	TRIGGER INPUTS. input signals 0V/5V. Active at the falling edge of the signal.

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TEST & CALIBRATION PROCEDURE
MUX ADC BOARD 7001E9313-27

MCS/OCS - 2000

Part number: 0692E9310-25

From : SEE engineering - K. Stam
Ref .nr : PC
Date : 0394
ERN : 1124
ECN : --
Rev : A

Checked : Peter Tel Date : 31. 3. 94

Approved : Date : 31.3.94

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TESTING

EQUIPMENT:

TESTCONNECTOR IPTE E9407-01
SERVICE DISK VERSION V5.0 OR HIGHER

1./ **After calibration turn** off the bower and connect the **connector IPTE E9407-01 in socket J1, J2 and TP1.**

2./ **Start up the system with the service** disc.

3./ **Select the** "FACTORY TEST" **menu, press the '#' key until the** "FACTORY TEST" menu is reached. Select **the "DIGITAL RACK TEST" menu. Select the "MUX ADC BOARD". Check that with an amplification of X1, the number of ZERO counts is 0 ± 44. Check also that with an amplification of X1, the number of span counts is 2003 ± 44. Note that the conversion time is about 96 μs.**

4./ **Go back to the "FACTORY TEST" menu and select the** "ANALOG RACK TEST". **Select the "BOOM POD" Check that the** 'VOLTAGE READ' **of KL. 1 is 0.0000 ± 0.008 VDC. Check also that the 'VOLTAGE READ' of KL. 15 is 7.350 ± 0.008 VDC.**

5./ **Testing. complete**

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CALIBRATION

EQUIPMENT:	DESCRIPTION:
DVM	41/2 DIGIT DVM OR EQUIVALENT

1./ **Insert the MUX ADC board into slot J20 and turn on the power of the MCS/OCS**

2./ **Measure with the DVM between TP1 and the GND LUG. The DVM reading should be 7.350 ± 0.001 VDC = = > Adjust with RV2**

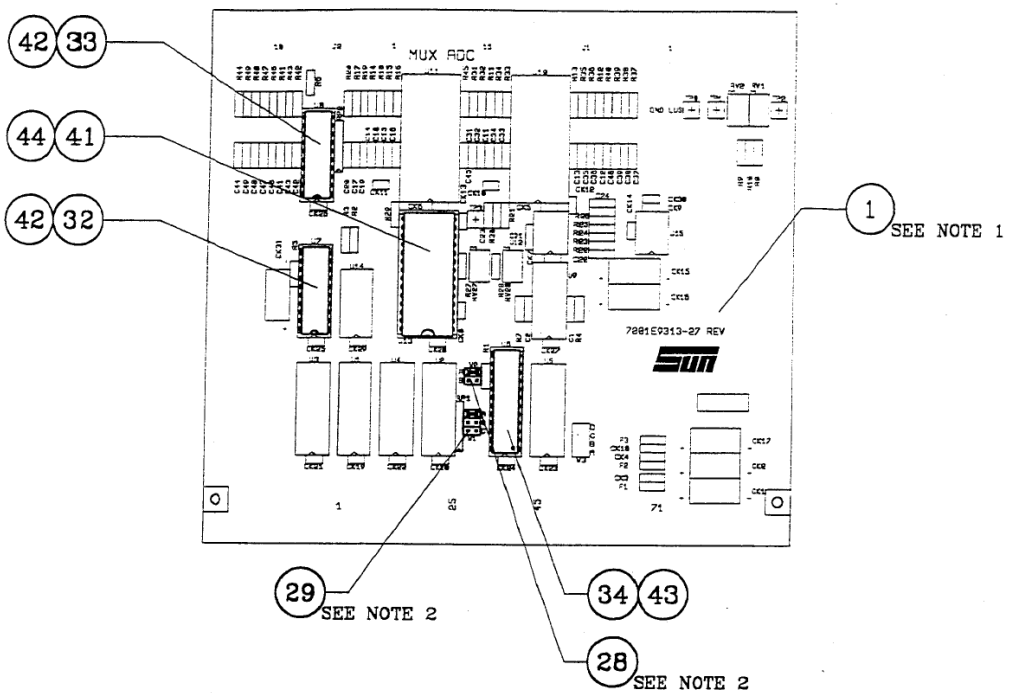
3./ **Measure with the DVM between TP2 and the GND LUG. The DVM reading should be 1.8375 ± 0.0005 VDC = = > Adjust with RV1**

4./ **Calibration complete**

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Revisions			
Revi	Date	Description	Check / Appr.
A	03'94	ERN 1124 R.F.P.	P.T. / BG



30	1/12	7096E3055-91	JUMPERSTRIP DOUBLE 3 POS	W1
29	1/18	7096E3055-91	JUMPERSTRIP DOUBLE 2 POS	W2
28	1	0679-0453-00	CAP. 100µF 50V elec ax	CK17
27				CK16,CK31
26	5	0679-1256-00	CAP. 10µF 35V elec ax	CK1,CK2,CK15,
25				C31-C49
24				C11-C20,C22,
23	55	0860-0180-08	CAP. 100nF 50V cer ax	C3-C14,C18-C30
22	1	7096E1080-32	CAP. 10nF 50V cer ax	C1
21	1	0860-0179-25	CAP. 1nF 100V cer ax	C24
20	1	0860-0179-17	CAP. 220pF 100V cer ax	C2
19	2	0860-0179-04	CAP. 18pF 100v cer ax	C21,C23
18	1	0668-0901-00	RESISTOR ZERO OHM	R22
17	2	0685-0448-08	POTMTR PC MNT (25 TURN)	RV1,RV2
16	2	7096E0085-14	RES. NETWORK 5*10K	RP1,RP2
15	1	1670-3304-00	RES. 33K 0.25W 1%	R30
14	2	1670-2214-00	RES. 22K1 0.25W 1%	R2,R3
13	1	1670-1744-00	RES. 17K4 0.25W 1%	R4
12	1	1670-1074-00	RES. 10K7 0.25W 1%	R9
11	1	1670-6493-00	RES. 6K49 0.25W 1%	R7
10	1	1670-5113-00	RES. 5K11 0.25W 1%	R10
9	1	1670-4993-00	RES. 4K99 0.25W 1%	R25
8	2	1670-4703-00	RES. 4K7 0.25W 1%	R21,R29
7	1	1670-3483-00	RES. 3K48 0.25W 1%	R8
6	1	1670-2213-00	RES. 2K21 0.25W 1%	R24
5	29	1670-2003-00	RES. 2K 0.25W 1%	R11-R20,R31-R49
4	1	1670-1693-00	RES. 1K69 0.25W 1%	R28
3	3	1670-1002-00	RES. 100E 0.25W 1%	R1,R5,R6
2	2	1670-4991-00	RES. 49E9 0.25W 1%	R27,R28
1	1	7025E9313-27	PCB MUX ADC BOARD	
Item	Qty.	Dwg./Part no.	Description	Remarks

Scale	N.T.S.	Date	Used in MCS/OCS
Designed by	KEES STAM	03-94	Material
Drawn by	R. V/D HOEF	03-94	
Checked by	Peter Tel	31.3.94	
Approved	B. Gee	31.3.94	Finish

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±01 Rest ±0.5
Remove all sharp corners and remove burns

Description	PCB ASSY MUX ADC	Dwgno	7001E9313-27
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		Project no.	

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51	REF	0692E9310-25	TEST & CAL. PROC. MUX ADC BD.	
50	REF	0692E9310-24	FUNC. DESC. MUX ADC BD	
49	REF	7092E9313-27	SCHEMATIC MUX ADC BOARD	
48				
47	1	0681-0802-06	CARD EXTRACTOR	
46	4	7096E7075-02	TEST BUTTON	TP0,TP1,TP2,TP3
45	3	0739-0106-07	PICO FUSE 1A	F1,F2,F3
44	1	7096E3056-07	IC SOCKET 28 PINS	U13
43	1	7096E3056-05	IC SOCKET 24 PINS	U6
42	2	7096E3056-04	IC SOCKET 20 PINS	U7,U8
41	1	7096E2080-64	IC HADC574ZBC	U13
40	5	7096E2080-59	IC 74HCT541	U1,U2,U3,U4,U5
39	2	7096E2070-25	IC ADG526	U10,U11
38	1	7096E2070-24	IC AD712JN	U12
37	1	7096E2070-22	IC DG419	U15
36	1	0773-8014-00	IC 74HCT4538	U9
35	1	0773-6901-00	IC 74C901	U14
34	1	0733E0551-64	DECODER GAL (MUX ADC)	U6
33	1	0733E0571-64	TRIGGER GAL (MUX ADC)	U8
32	1	0733E0561-64	CONTROL GAL (MUX ADC)	U7
31	2	7096E3055-12	JUMPER	W1,W2

NOTE:
1) ADD CURRENT REVISION LEVEL
2) JUMPER SETTINGS
   W1: A INSTALLED
       B NOT INSTALLED
       C NOT INSTALLED
   W2: A INSTALLED
       B NOT INSTALLED
   W3: A DEFAULT IN COPPER
       B NOT INSTALLED
       C NOT INSTALLED
       D NOT INSTALLED

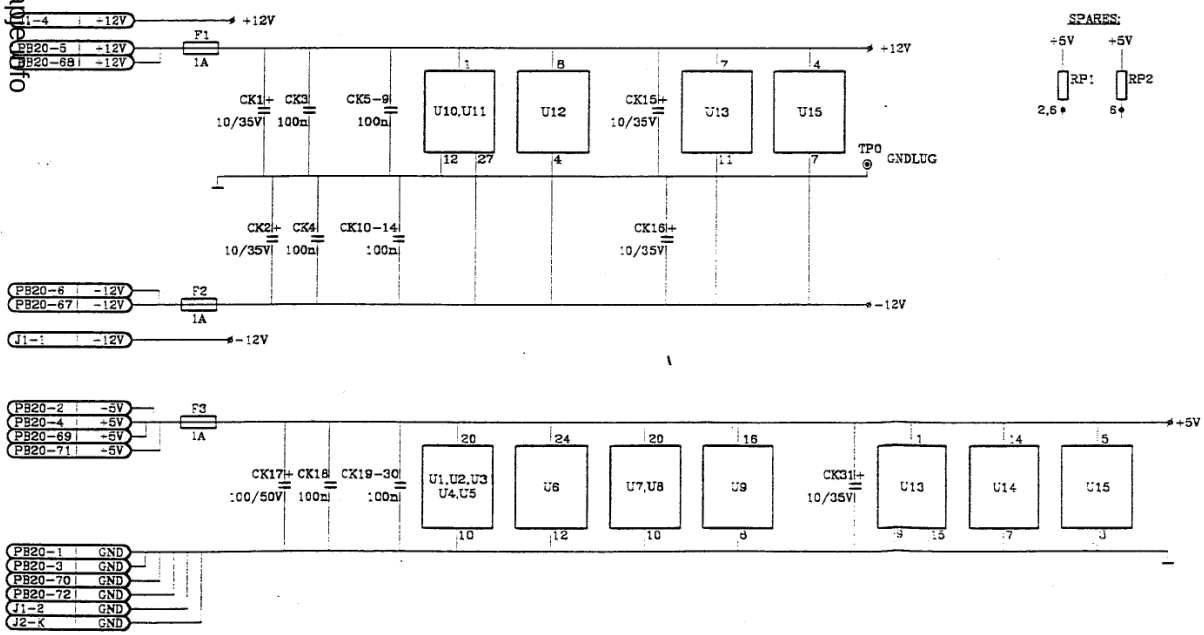
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Issue	Print Date	Description	Check	Appr.
A	03'94	ERN 1124 R.F.P.	P.T.	BG

PB20 CONNECTOR			
PIN NO	SIGNAL	PIN NO	SIGNAL
1	GND	37	BA7
2	+5V	38	N.C.
3	GND	39	BA8
4	+5V	40	N.C.
5	-12V	41	N.C.
6	-12V	42	N.C.
7	N.C.	43	N.C.
8	N.C.	44	N.C.
9	BD0	45	N.C.
10	BD8	46	N.C.
11	BD1	47	N.C.
12	BD9	48	CLK 4M
13	BD2	49	N.C.
14	BD10	50	N.C.
15	BD3	51	/INT5
16	BD11	52	/INT3
17	BD4	53	/INT4
18	BD12	54	/INT2
19	BD5	55	N.C.
20	BD13	56	N.C
21	BD6	57	/INIT
22	BD14	58	N.C.
23	BD7	59	N.C.
24	BD15	60	N.C.
25	N.C.	61	N.C.
26	BA9	62	IORD
27	N.C.	63	N.C.
28	BA10	64	IOWR
29	N.C.	65	N.C.
30	N.C.	66	N.C.
31	N.C.	67	-12V
32	N.C.	68	+12V
33	BA5	69	+5V
34	N.C.	70	GND
35	BA6	71	+5V
36	N.C.	72	GND

J1 CONNECTOR			
PIN NO	SIGNAL	PIN NO	SIGNAL
1	-12V	A	CHANNEL 24
2	GND	B	P SIG
3	N.C.	C	VACU
4	-12V	D	ATEMP
5	N.C.	E	CO2 ANA
6	PRIM AVAIL	F	O2 ANA
7	CHANNEL 14	H	HC ANAH
8	AVE AMP	J	O2 SIG
9	CHANNEL 16	K	BATT ANA
10	CHANNEL 9	L	CHANNEL 12
11	TEMP. ANA	M	RAW AMPS
12	VAC ANA	N	KL1 ANA
13	V/Q ANA	P	N.C.
14	CHANNEL 4	R	/DELAYED DWELL
15	CYL. CLOCK	S	TRIGGER 4

J2 CONNECTOR			
PIN NO	SIGNAL	PIN NO	SIGNAL
1	O2 SIG	A	SPK 2kV
2	HC ANAH	B	PK kV
3	O2 ANA	C	RIPPLE VOLT
4	CO2 ANA	D	HC ANA L
5	ATEMP	E	CO ANA
6	VACU	F	SEC AVAIL
7	P SIG	H	KL15 ANA
8	CHANNEL 24	J	SPK 1 kV
9	TRIGGER 7	K	GND
10	TRIGGER 6	L	TRIGGER 5



NOTES:

1) UNLESS OTHERWISE SPECIFIED
   A) ALL RESISTORS ARE IN OHMS.1/4W.1%
   B) ALL CAPACITORS ARE IN MICRO-FARADS
   C) ALL DIODES ARE 1N914 OR 1N4148
   D) ALL IC'S ARE 74HCT-SERIES TYPE
   E) ALL POLARIZED CAPACITORS ARE 16V
2) LAST USED NO'S: R49, RV28, C49, U15, F3, CK31, W3, TP3.
3) NOT USED NO'S: C3-C10, RV3-RV26.
4) COMPONENTS MARKED WITH ■ ARE NOT INSTALLED
5) JUMPER SETTINGS
   W1: A INSTALLED
       B NOT INSTALLED
       C NOT INSTALLED
   W2: A INSTALLED
       B NOT INSTALLED
   W3: A DEFAULT IN COPPER
       B NOT INSTALLED
       C NOT INSTALLED
       D NOT INSTALLED
6) CAPACITORS MARKED WITH * ARE 100nF

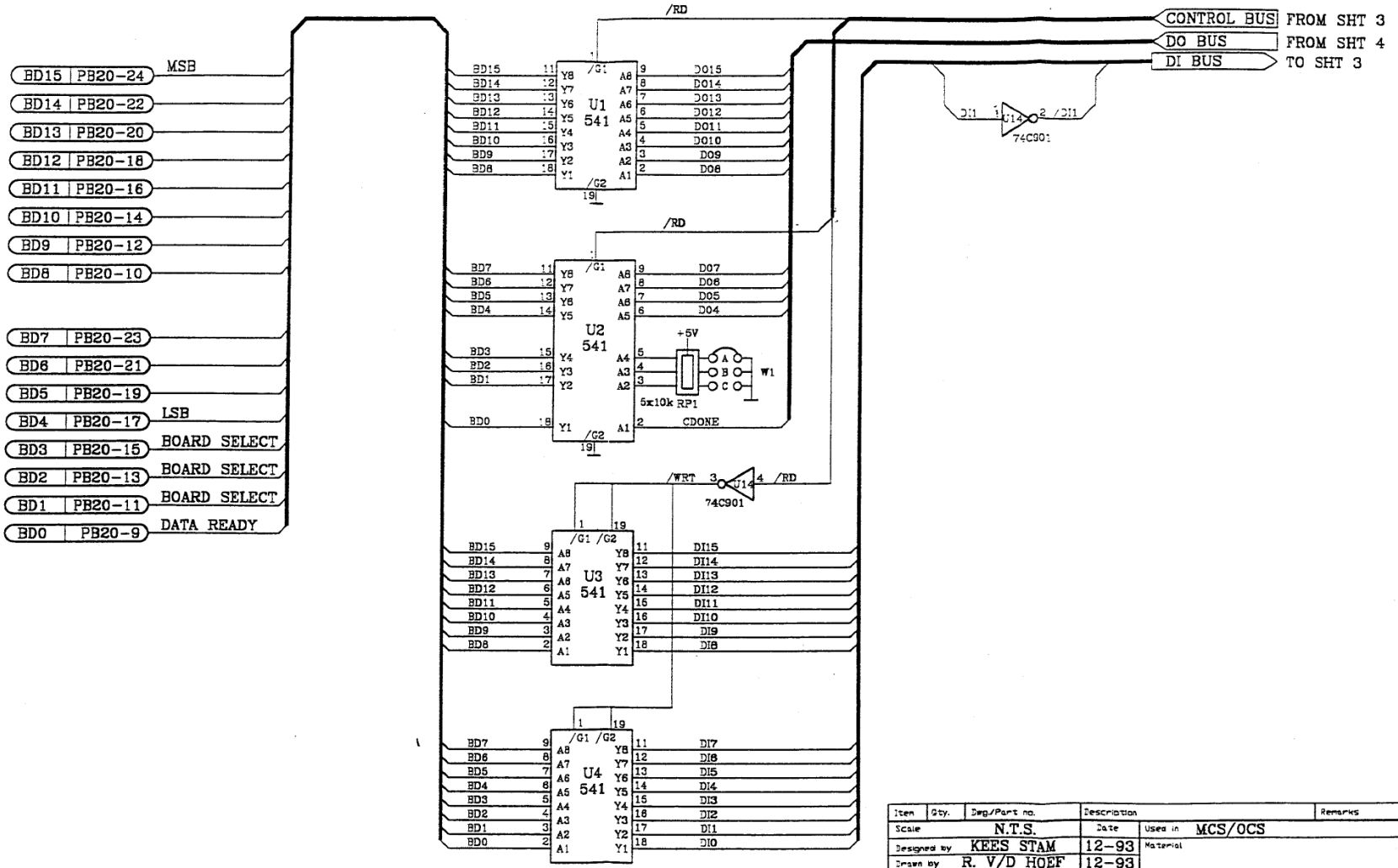
Item	Qty.	Dwg/Part no.	Description	Remarks
Scale	N.T.S.	Date	Used in MCS, OCS	
Designed by	KEES STAM	01-94	Material	
Drawn by	R. V/D HOEF	03-94		
Checked by	Peter Tel	3.3.94		
Approved		31.3.94		

Unless otherwise specified: Dimensions are in mm; Tolerances on: Angles ±5°, Holes ±0.1, Bend ±1.5
Remove all sharp corners and remove burrs

Description	Drawing
SCHEMATIC MUX ADC BOARD	7092E9313-27

SIS ELECTRONIC ATOMIC B.V. | A1 | Sheet 1 of 4 | Project no. | Rev. A

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Item	Qty.	Dwg./Part no.	Description		Remarks
Scale	N.T.S.		Date	Used in	MCS/OCS
Designed by	KEES STAM		12-93	Material	
Drawn by	R. V/D HOEF		12-93		
Checked by	Peter Tel		31.3.94		
Approved	R. Lee		31.3.94	Finish	

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±0.1 Rest ±0.5

Remove all sharp corners and remove burrs

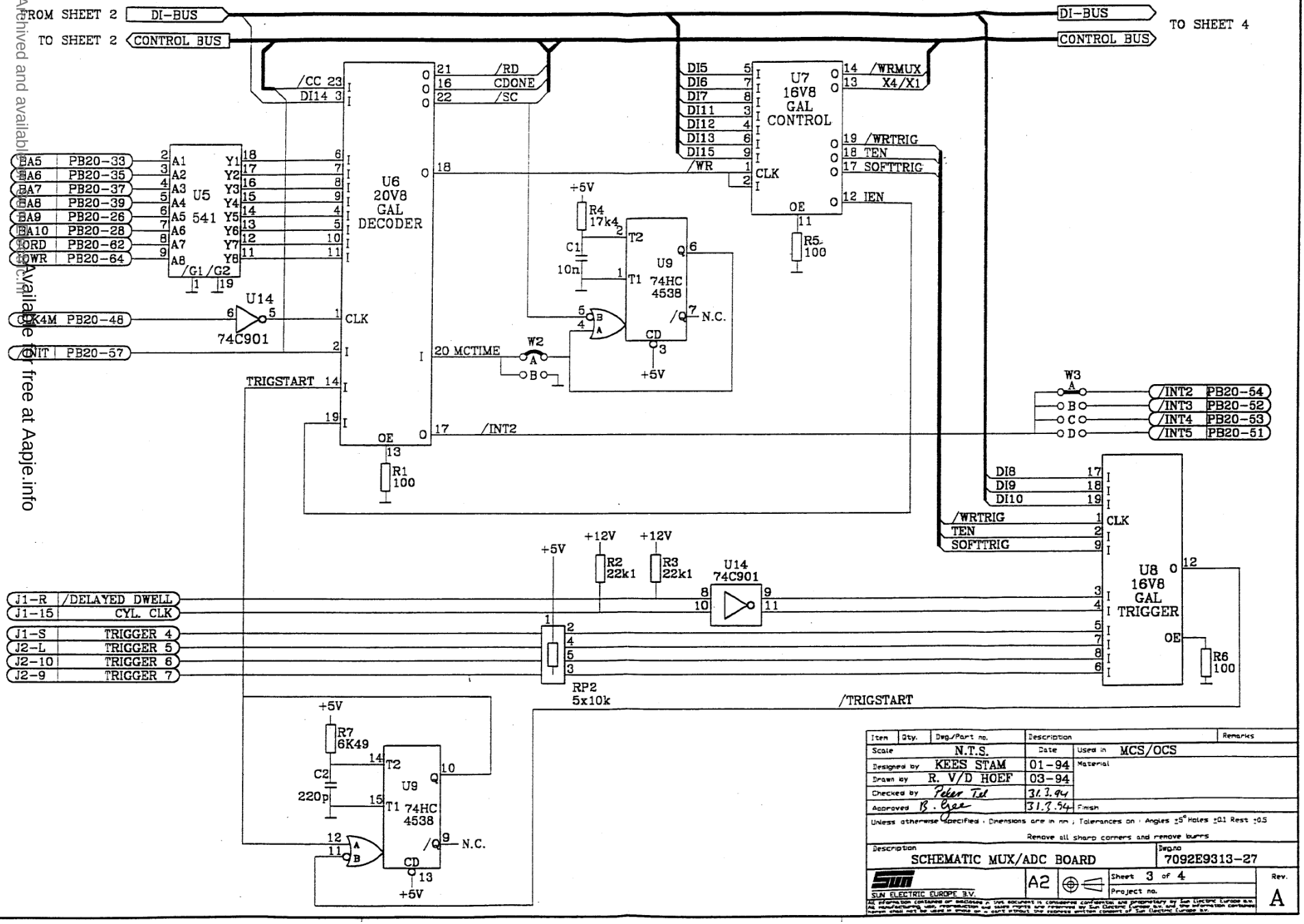
Description: SCHEMATIC MUX ADC BOARD

Dwg.no: 7092E9313-27

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Item	Qty.	Dwg./Part no.	Description		Remarks
Scale	N.T.S.		Date	Used in	MCS/OCS
Designed by	KEES STAM		01-94	Material	
Drawn by	R. V/D HOEF		03-94		
Checked by	Peter Tel		31.3.94		
Approved	B. Gee		31.3.94	Finish	

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±0.1 Rest ±0.5

Remove all sharp corners and remove burrs

Description: SCHEMATIC MUX/ADC BOARD

Dwg.no: 7092E9313-27

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A2

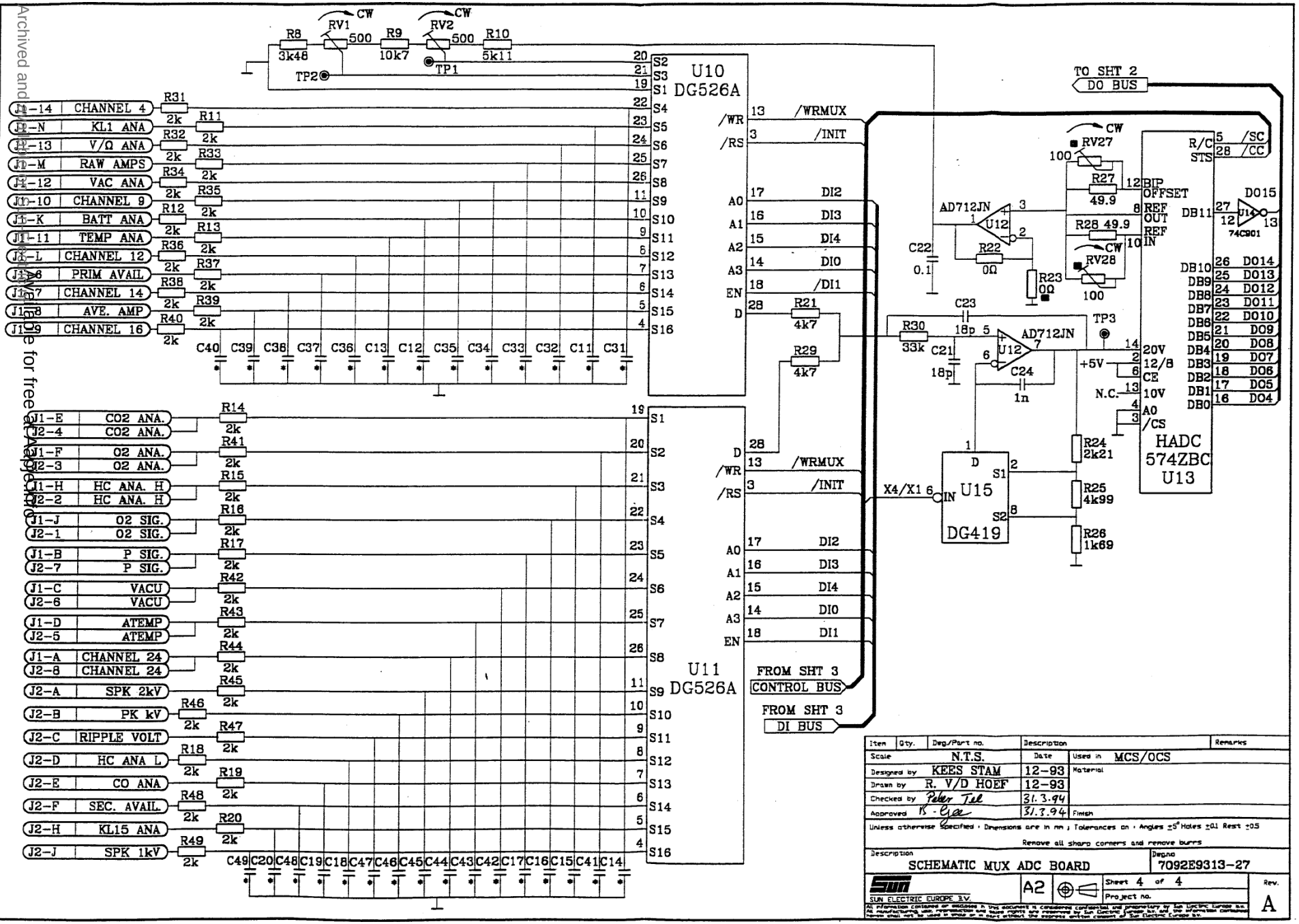
Sheet 3 of 4

Project no.

Rev. A

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Item	Qty.	Dwg./Part no.	Description	Remarks
Scale	N.T.S.	Date	Used in MCS/OCS	
Designed by	KEES STAM	12-93	Material	
Drawn by	R. V/D HOEF	12-93		
Checked by	Peter Tel	31.3.94		
Approved	K-Gea	31.3.94	Finish	

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±01 Rest ±05

Remove all sharp corners and remove burrs

Description: SCHEMATIC MUX ADC BOARD

Dwg.no: 7092E9313-27

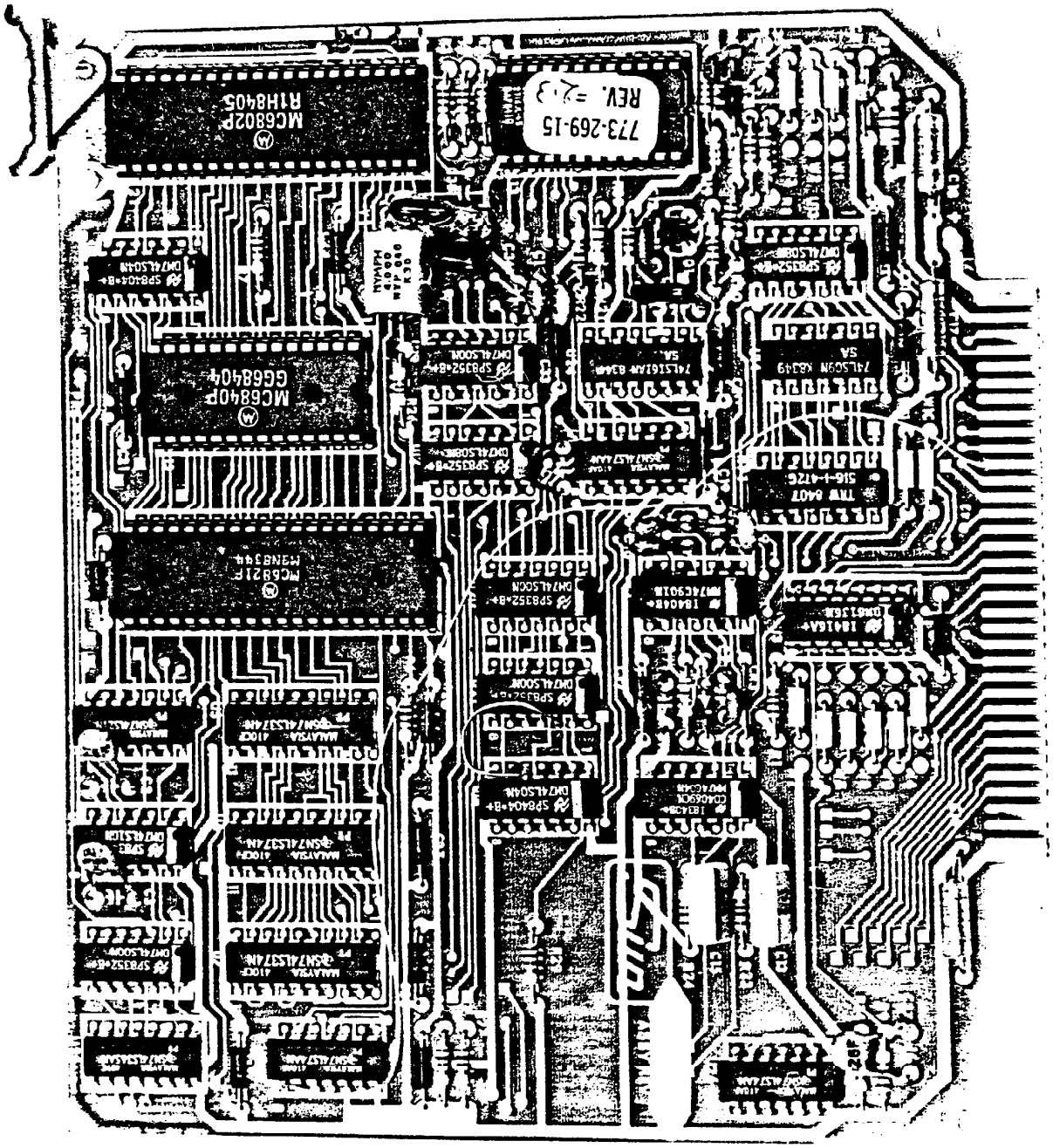
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3.1.9

PRE-PROCESSSORBD. (SLOT 10)



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B. PRE-PROCESSOR BD.(SLOT 10)

THE PRE-PROCESSOR BOARD IS USED BY THE CPU BOARD AND CYLINDER SHORTING CIRCUITRY. INSTEAD OF HARD LOGIC (GATES, COUNTERS ETC), THE BOARD UTILIZES A MICROPROCESSOR TO PROCESS THE INCOMING SIGNALS. ALL SUPPORT CIRCUITRY. INCLUDING CLOCK, RAM, ROM AND INPUT/OUTPUT IS TOTALLY CONTAINED ON THE BOARD. DO NOT CONFUSE THIS PROCESSOR WITH THE ONE ON THE CPU BOARD. THE PRE-PROCESSOR'S CPU IS A SLAVE TO THE CPU BOARD.

USING THE INPUTS AT J811 (ON THE BACKPLANE), THE PRE-PROCESSOR BOARD IS RESPONSIBLE FOR CONTINUOUSLY CALCULATING RPM, DWELL AND TIMING DATA. THE CPU BOARD MAY AT ANY TIME REQUEST THE DATA FOR ANY OF THESE PARAMETERS VIA THE DIGITAL BACKPLANE BUSSES. THE CPU BOARD TRANSFORMS THE BINARY DATA RECEIVED INTO A FORM SUITABLE FOR DISPLAY. THE PRE-PROCESSING OF THESE PARAMETERS FREES THE CPU BOARD TO PERFORM OTHER DUTIES.

INPUTS

CYL CLOCK PIN 44--FROM TRIGGER BOARD (SLOT 12) PIN 9.
(J811 PIN 3) THE FALLING EDGE COINCIDES WITH POINT OPEN OF EACH CYLINDER.

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INPUTS CONT.

ENG SYNC (J811 PIN 8) — PIN 46--FROM TRIGGER BOARD (SLOT 12) PIN 14.
THE FALLING EDGE COINCIDES WITH POINT OPEN OF THE # 1 CYLINDER.

DELAYED DWELL (J811 PIN 4) — PIN 50--FROM TRIGGER BOARD (SLOT 12) PIN 11.
DELAYED LOW NOISE VERSION OF CYL.CLOCK. GOES HIGH FOR A TIME PROPORTIONAL TO DWELL.

MON (J811 PIN 9) — PIN 41--FROM TIMING BOARD (SLOT 7) PIN D.
GOES LOW TO INFORM THE PRE-PROCESSOR THAT THE TIMING SIGNAL IS BEING PRODUCED BY A DOMESTIC TIMING PROBE.

TIMING PULSE (J811 PIN 6) — PIN 48--FROM TIMING BOARD (SLOT 7) PIN 7.
FALLING EDGE OF PULSE, RELATIVE TO ENG SYNC, IS PROPORTIONAL TO TIMING. THE PULSE IS POSITIVE GOING WHEN IN MAGNETIC TIMING OR IN THE "TIME" STROBOSCOPIC MODES. THE PULSE IS NEGATIVE GOING IN THE "0" STROBOSCOPIC MODE.

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THE PRE-PROCESSOR ALSO OUTPUTS A SIGNAL FOR USE BY THE ANALOG RACK TO INITIATE CYLINDER SHORTING.

OUTPUTS

SELECTED CYLINDER (J811 PIN 6)	PIN 45--TO MISCELANEOUS FUNCTION BD (SLOT 11) PIN 11; GOES HIGH FROM POINT CLOSE OF THE CYLINDER PRECEEDING THE SELECTED CYLINDER TO POINT CLOSE OF THE SELECTED CYLINDER.

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3.2 DISC DRIVE

3.2.1 GENERAL

3.2.22 DRIVE SPECIFICATION

3.2.3 INTERFACE

3.2.4 CONNECTOR/SIGNAL LOCATIONS

3.2.5 OPERATING PROCEDURES

3.2.6 MAINTENANCE

3.2.1 GENERAL

THE FD1036 MICRO-FLOPPY DISC DRIVE IS A DOUBLE-SIDED MICRO-FLOPPY DISC DRIVE WITH 135 TRACKS PER INCH (TPI).

THE MICRO-FLOPPY DISC (ABBREVIATED AS DISC IN THIS MANUAL) USED FOR FD1036 IS CONTAINED IN A HARD JACKET WITH AUTO SHUTTER.

THE FD1036 MICRO-FLOPPY DISC DRIVE HAS A TOTAL VOLUME ONE FOURTH THAT OF CONVENTIONAL 5-1/4* MINIFLOPPY DISC DRIVES AND WEIGHTS ONLY APPROXIMATELY 560 G. YET HAS A COMPARABLE STORAGE CAPACITY.

THE DRIVE USES A DIRECT-DRIVEN SPINDLE WITH A BRUSHLESS DC MOTOR, AND BY DUE THE LOW POWER DESIGN IT CONSUMES ONLY 2.1 WATTS OF POWER (TYP).

THE LOW NOISE DESIGN ASSURES SILENT OPERATION.

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3.2.2 DRIVE SPECIFICATION

No.	ITEM		SPECIFICATION		UNIT
1	RECORDING MODE		MFM	FM	
2	CAPACITY	UNFORMATTED	1	0.5	MB
		FORMATTED (NOTE1)	640	320	kB
3	DATA TRANSFER RATE		250	125	kBIT/sec
4	MAXIMUM BIT DENSITY		8717.	4359	BPI
5	TRACKS		160		
6	AVERAGE ROTATIONAL SPEED		300		RPM
7	SEEK TIME (TRACK-TO-TRACK)		3		ms
8	SEEK SETTLING TIME		15		ms
9	TRACK DENSITY		135		TPI
10	START TIME (NOTE 2)		800		ns
11	STANDARD EXTERNAL DIMENSIONS (NOTE 3)	WIDTH	30 (1.2)		mm (in)
		HEIGHT	101.6 (4)		mm (in)
		DEPTH	146 MAX (5.75)		mm (in)
12	WEIGHT		560		gr
13	OPERATING ENVIRONMENT CONDITIONS	TEMPERATURE	5 - 45		°C
		RELATIVE HUMIDITY	20 - 80		%RH
		MAX. WET-BULB TEMP.	29.0 (NO BEDEWING)		°C

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No	ITEM		SPECIFICATION		UNIT
14	POWER SUPPLY REQUIREMENT	VOLTAGE (V)	STAND-BY CURRENT (NOTE4)	STEADY STATE CURRENT (NOTE5)	
		+12v	LESS THAN 0.1	90	mA
		+5v	60	200	mA
15	POWER DISSIPATION		0.3	2.1	W
16	HEAT OUTPUT		0.26	1.8	kcal/h
17	RELIABILITY	MTBF (NOTE 6)	12000 (UNDER STANDARD USE CONDITIONS)		POH
		MTTR	0.5		h
		DEVICE LIFE	15000 POH or 5 YEARS (DESIGN LIFE)		
		SOFT ERRORS	10^{-9} (NOT INCLUDING 2 OR LESS RETRY ATTEMPS)		TIMES/BIT
		HARO ERRORS	10^{-12}		TIMES/BIT
		SEEK ERROR RATIO	1 0 "		TIMES/ SEEK
18	DISK LIFE		3.0 x 10 6		PASS COUNT/ TRACK
19	DISK		DOUBLE SIDED 3.5 DISKETTE SPEC. BY NEC		
20	DRIVE ENVIRONMENT	OPERATING	NON-OPERATING (STORAGE1	TRANSPORTING (PACKING)	UNIT
	TEMPERATURE	4 - 46 (39 - 115)	-20~50 (4 ~122)	-40~ 60 (-40 ~ 140)	°C (F)
	RELATIVE HUMIDITY	20 - 80	10 ~ 90	5~ 95	%RH
	MAX-WET-BULB TEMPERATURE	29 (84)	40 (104)	45 (113)	°C (F)
	LARGEST TEMPERATURE	20 (59)	30 (86)	30 (86)	°C/h (°F/h)

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NOTE 1 : 16 SECTORS/TRACK, 256 BYTES/SECTOR TIME

2 : TIME UNTIL "READY" AFTER "MOTOR ON"

3 : DIMENSIONS NOT INCLUDING THAT OF THE FRONT BEZEL

4 : IF THE MEDIUM IS NOT INSERTED OR THE "MOTOR ON" SIGNAL IS INVALID

5 : WHEN FDD IS IN "READY" STATUS

6 : UNDER STADARD USE CONDITIONS

(1) DRIVE SERVICE TIME (POH) : 8 H/DAY

(2) ACTUAL HEAD LOAD TIME (R/W TIME) : 0:5 H/DAY

(3) DISC INSERTION/ EJECTION : 25 TIMES/DAY

(4) MOTOR ON/OFF : 300 TIMES/DAY

(5) AVERAGE USE TIME PER DISC : 2 H/DAY (4 DISCS/DAY.DRIVE)

7 : EXCITATION IN THREE DIRECTIONS ONE R/W TEST BY OUR FDD TESTER FOR 0 TO 79 TRACK

8 : BETWEEN SG AND FG : 90 k0hm (DC)

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3.2.3 INTERFACE

FDD'S MAY BE CONNECTED TO THE CONTROLLER IN EITHER PARALLEL OR DAISY-CHAIN CONFIGURATION. THE NUMBER OF FDD'S WHICH CAN BE CONNECTED TO ONE CONTROLLER DEPENDS ON INDIVIDUAL SYSTEMS AND CONTROLLER. FOR DAISY-CHAIN CONNECTION, EACH CONTROLLER CAN CONTROL UP TO 4 FDD'S.

SIGNAL LINE TERMINATION RESISTORS ARE PROVIDED ON EACH FDD. THE BASIC FDD CONNECTION TO THE CONTROLLER IS SHOWN IN FIGURES 1 AND 2.

A) PARALLEL CONNECTION

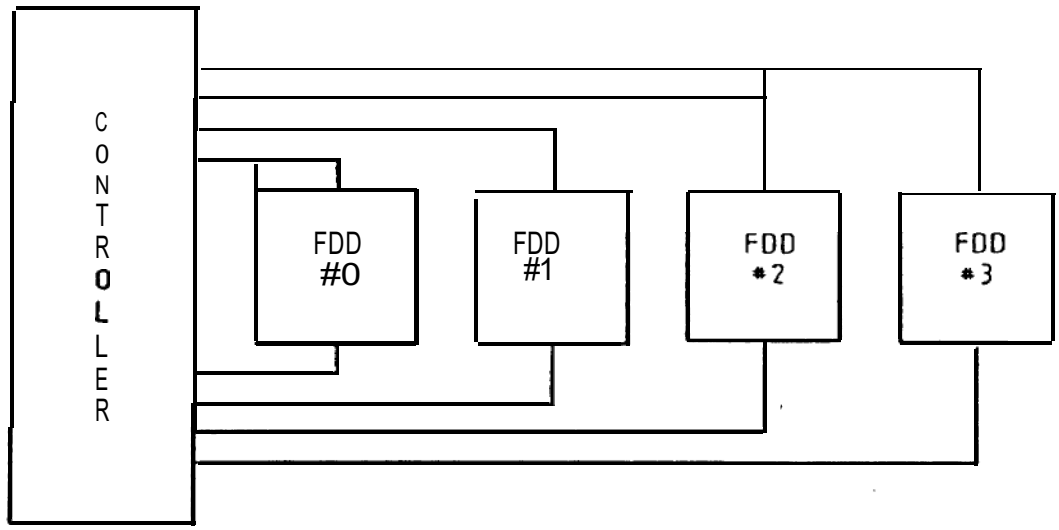


FIG. 1 SIGNAL CABLE MAXIMUM LENGTH 1 MTR.

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B) DAISY CHAIN CONNECTION

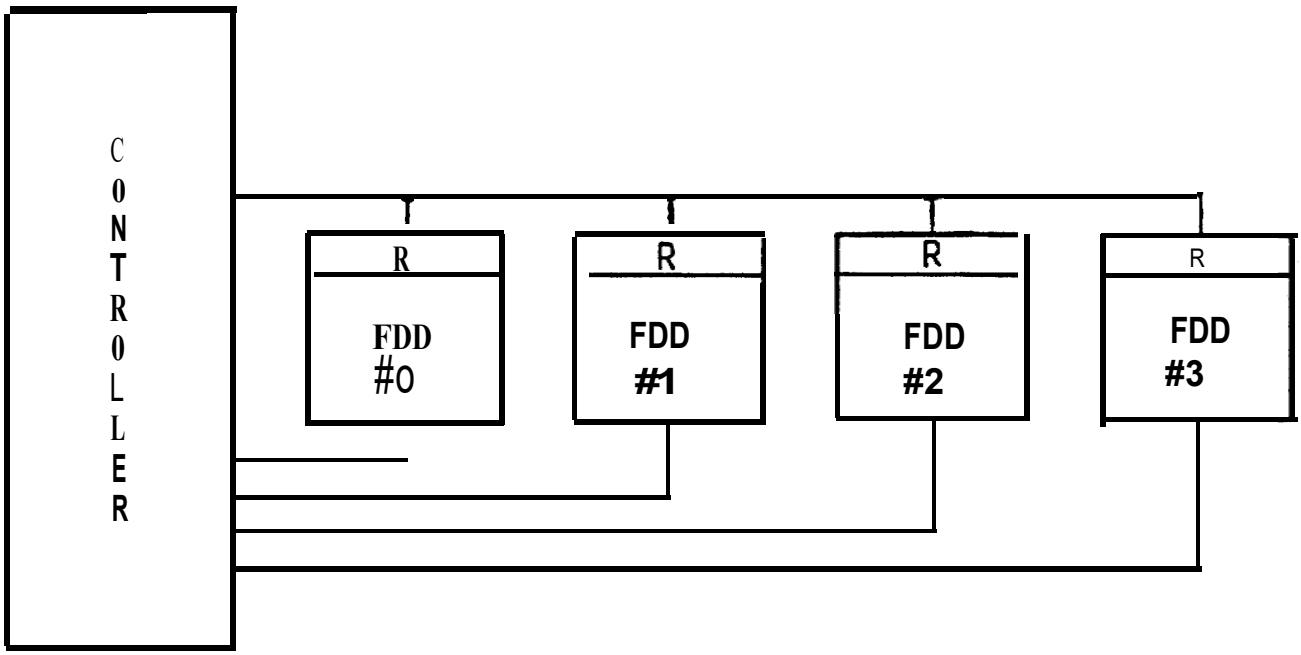


FIG. 2 SIGNAL CABLE MAXIMUM LENGTH 1 MTR.

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3.2.4 PHYSICAL SPECIFICATIONS

THE FDD IS CONNECTED TO ITS CONTROLLER THROUGH A SIGNAL CONNECTOR AND A POWER CONNECTOR. A FASTON TERMINAL IS PROVIDED FOR FRAME GROUND. THE CONNECTOR LOCATIONS ARE SHOWN IN FIGURE 1.

A) CONNECTOR LOCATIONS

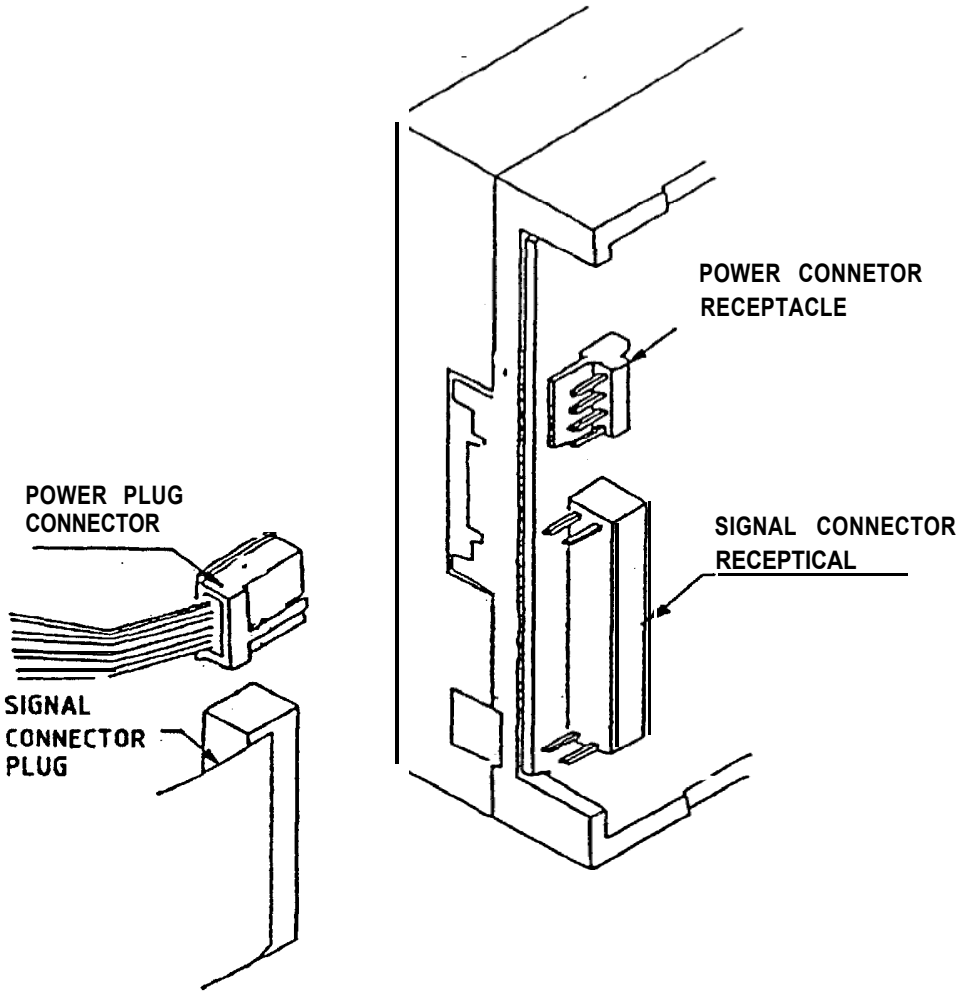
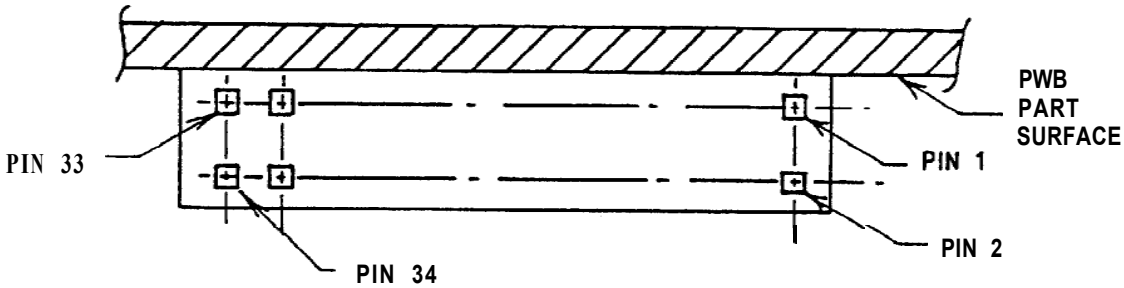


FIG. 1

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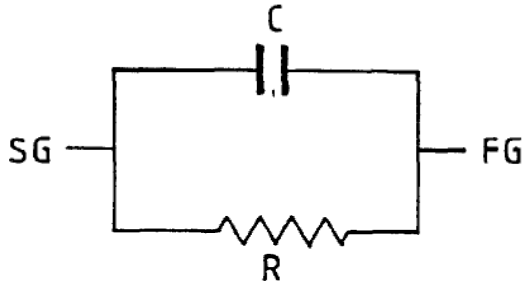
THE FOLLOWING SHOWS THE SIGNAL CONNECTOR PIN CONFIGURATION ON THE FD 1036 :



SIGNAL NAME	I/O SIGNAL	PIN NUMBER	PIN NUMBER	SIGNAL NAME
MOTOR ON 1		2	1	GND
IN USE	INPUT SIGNAL	4	3	GND
DRIVE SELECT 3	INPUT SIGNAL	6	5	GND
INDEX	OUTPUT SIGNAL	8	7	GND
DRIYE SELECT 0	INPUT SIGNAL	10	9	GND
DRIVE SELECT 1	INPUT SIGNAL	12	11	GND
DRIVE SELECT 2/ (MOTOR ON 1)	INPUT SIGNAL	14	13	GND
MOTOR ON	INPUT SIGNAL	16	15	GND
DIRECTION SELECT	INPUT SIGNAL	18	17	GND
STEP	INPUT SIGNAL	20	19	GND
WRITE DATA	INPUT SIGNAL	22	21	GND
WRITE GATE	INPUT SIGNAL	24	23	GND
TRACK 00	OUTPUT SIGNAL	26	25	GND
WRITE PROTECT	OUTPUT SIGNAL	28	27	GND
READ DATA	OUTPUT SIGNAL	30	29	GND
SIDE SELECT	INPUT SIGNAL	32	31	GND
READY	OUTPUT SIGNAL	34	33	GND

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FG AND SG PROCESSING AS FOLLOWS :

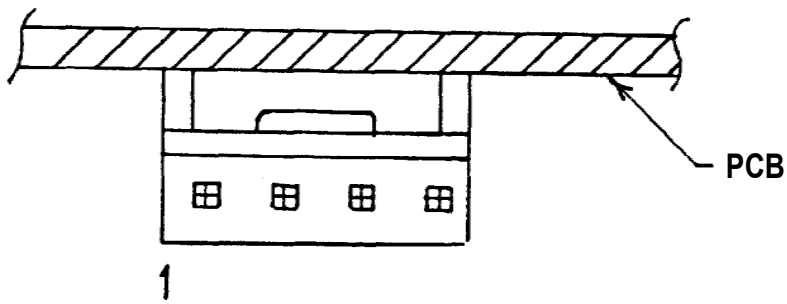


IMPEDANCE TERMINATOR

R = 100 K (± 10%), C = 0.1 μ F (- 40%) (+ 80%)

POWER CONNECTOR AND PIN CONFIGURATION

THE FOLLOWING SHOWS THE POWER CONNECTOR PIN CONFIGURATION :



POWER CONNECTOR IN CONFIGURATION

POWER CONNECTOR PIN ASSIGNMENTS

PIN NO.	SUPPLY, VOLTAGE.
1	+5V DC
2	GND
3	GND
4	+12V DC

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3.2.5 OPERATING PROCEDURES

THE BASIC OPERATING PROCEDURES FOR FDD INCLUDE :

A. SETTING A FLOPPY DISC

(1) INSERT THE DISKETTE SLOWLY INTO THE SLOT UNTIL THE EJECT BUTTON POPS OUT

B. REMOVING THE FLOPPY DISC

(1) MAKE SURE THE WRITE/READ OPERATION OF FDD HAS FINISHED
(2) TO EJECT THE DISKETTE FROM THE DRIVE, JUST PRESS THE EJECT BUTTON

C. DISPLAY LAMP

THE DISPLAY LAMP INDICATES THE FDD STATUS.
IT COMES ON WHILE HEADS ARE LOADED.

3.2.6 MAINTENANCE

DISC DRIVES ARE FACTORY ALIGNED.NO ATTEMPT SHOULD BE MADE TO ADJUST DISC DRIVES IN THE FIELD. IF A DRIVE IS SUSPECT REPLACE THE DRIVE.

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3.3 VDU ASSY

THE MCS 2000 VDU ASSY IS COMPATIBLE WITH THE MCS-2000 VDU.HOWEVER BOARD LAY-OUTS AND CIRCUIT DIFFERENCES HAVE OCCURED.

FOR ADJUSTMENT PROCEDURE SEE SECTION 2.

FOR CIRCUIT CHANGES SEE NEW SCHEMATICS IN SECTION 4.

THE VDU SHOULD BE TREATED AS AN INDIVIDUAL ITEM AND REPLACED AS SUCH IN THE FIELD.

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ANALOG RACK

3.41 GENERAL INFORMATION

3.42 TRIGGER PRIMARY BD.

3.43 TIMING BD.

3.44 VOLT/OHM BD.

3.45 KV PROCESSOR BD.

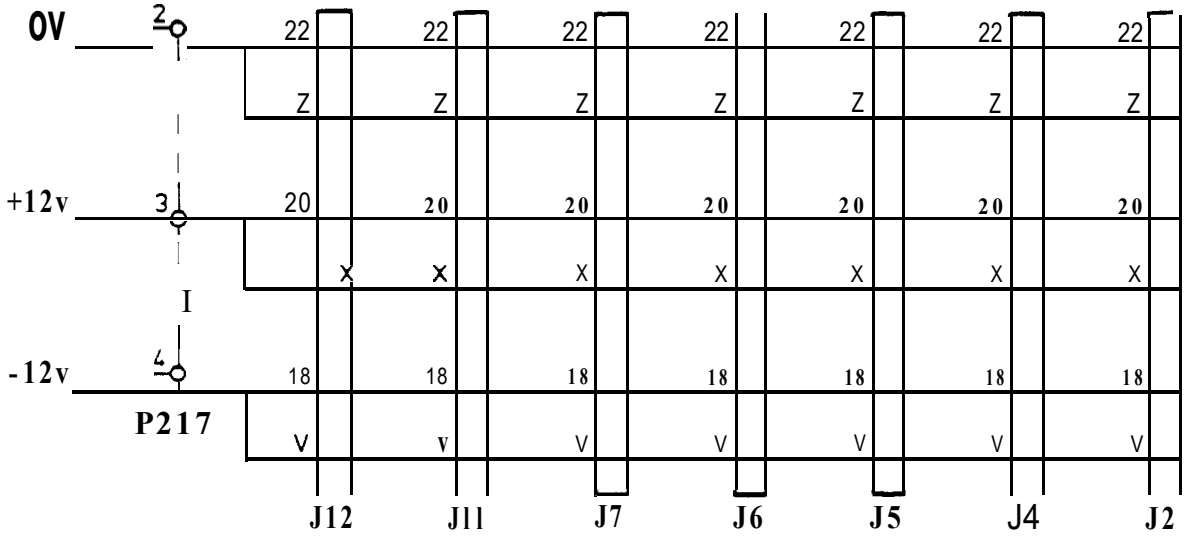
3.46 KV SLOPE BD.

3.47 MISC. FUNCTION BD.

3.48 AMP./TEMP. BD.

ANALOG RACK POWER SUPPLY 3.4.1

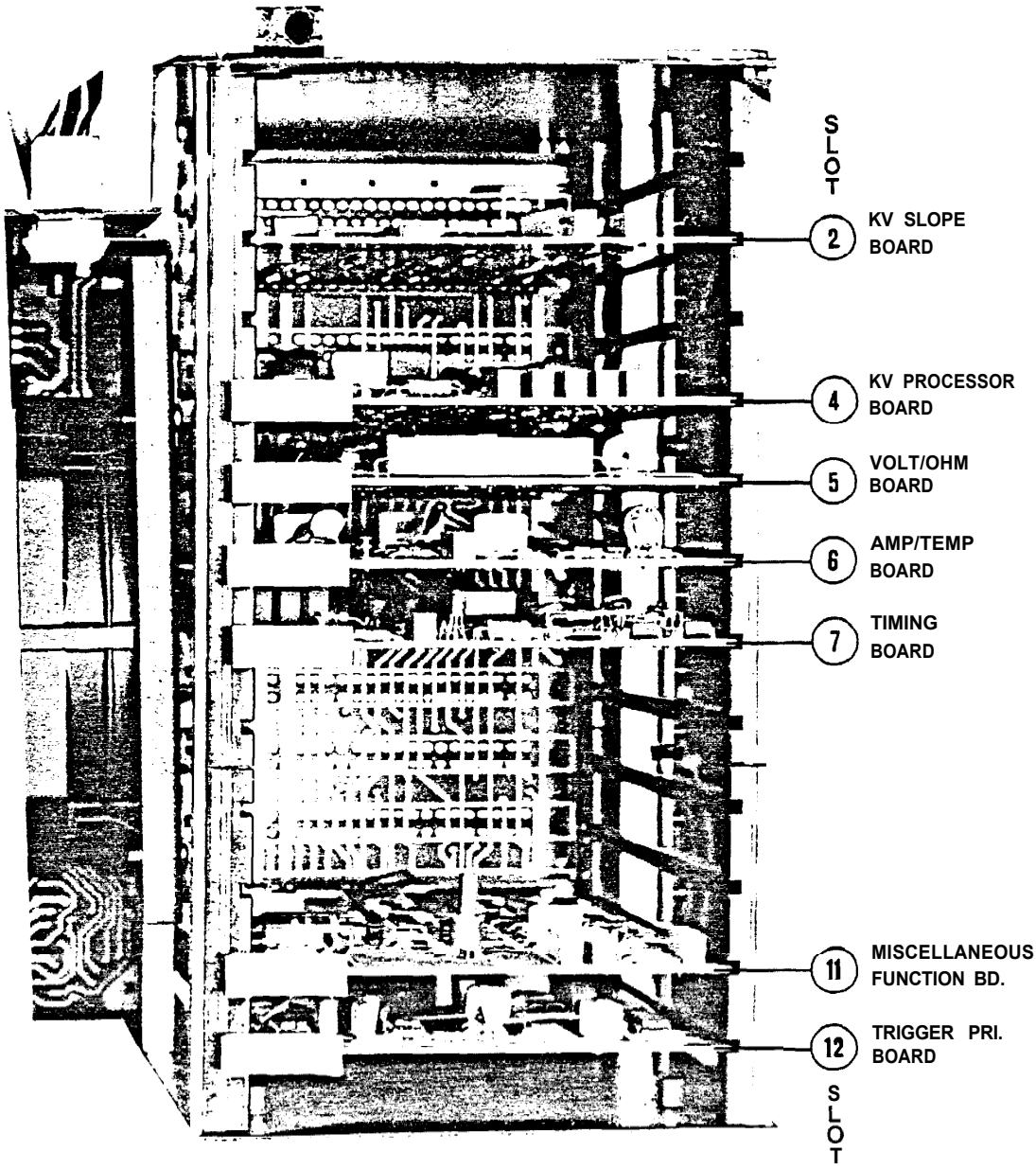
THE ANALOG RACK REQUIRES +12V, -12V AND 0V LINES TO OPERATE CORRECTLY. THESE SUPPLIES. ENTER THE ANALOG RACK AT P217 AND ARE DISTRIBUTED ON THE BACK PLANE AS FOLLOWS.



FOR THE GENERATION OF THESE SUPPLIES SEE SECTION 2 POWER SUPPLY AND DISTRIBUTION.

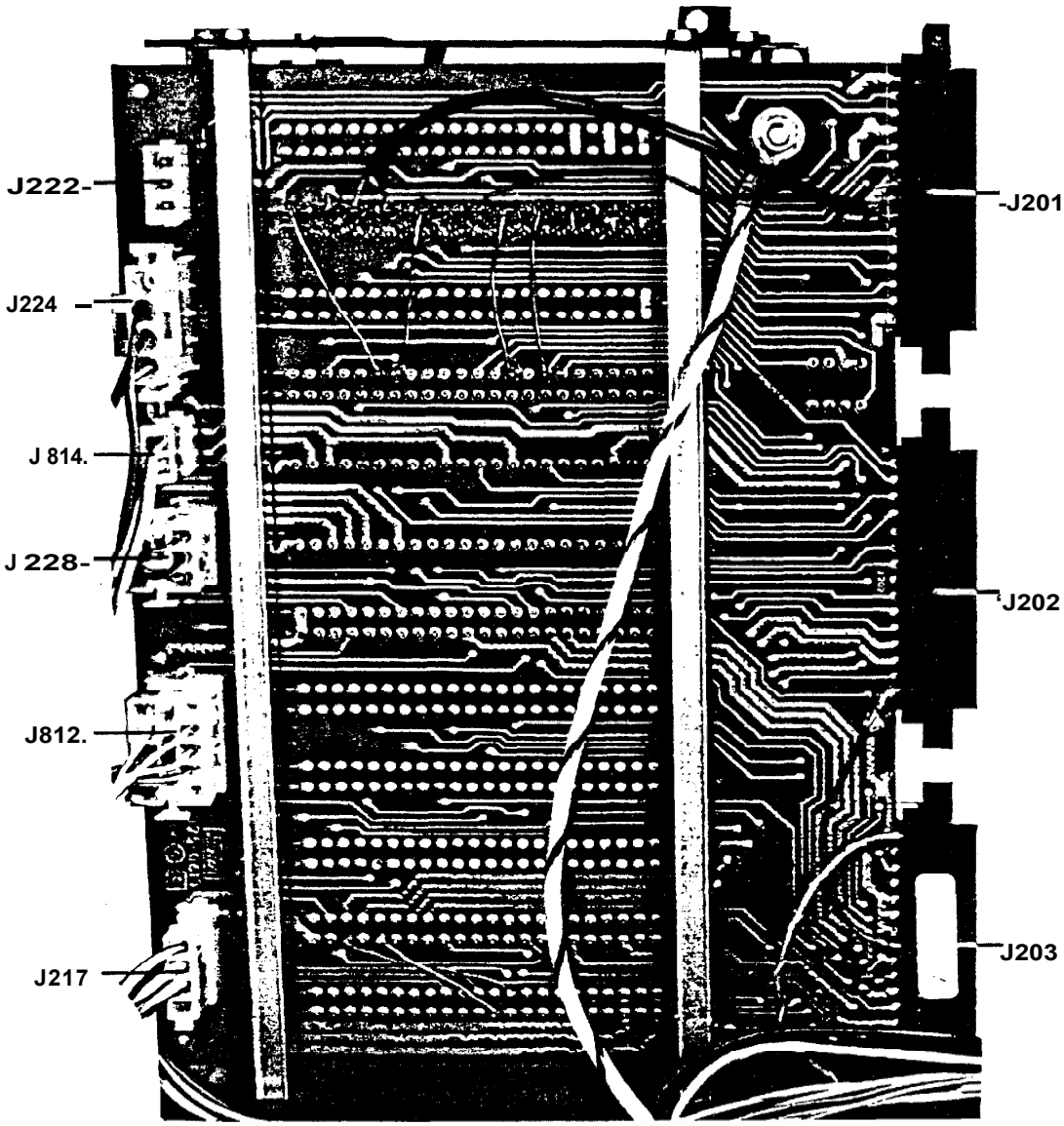
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ANALOG RACK



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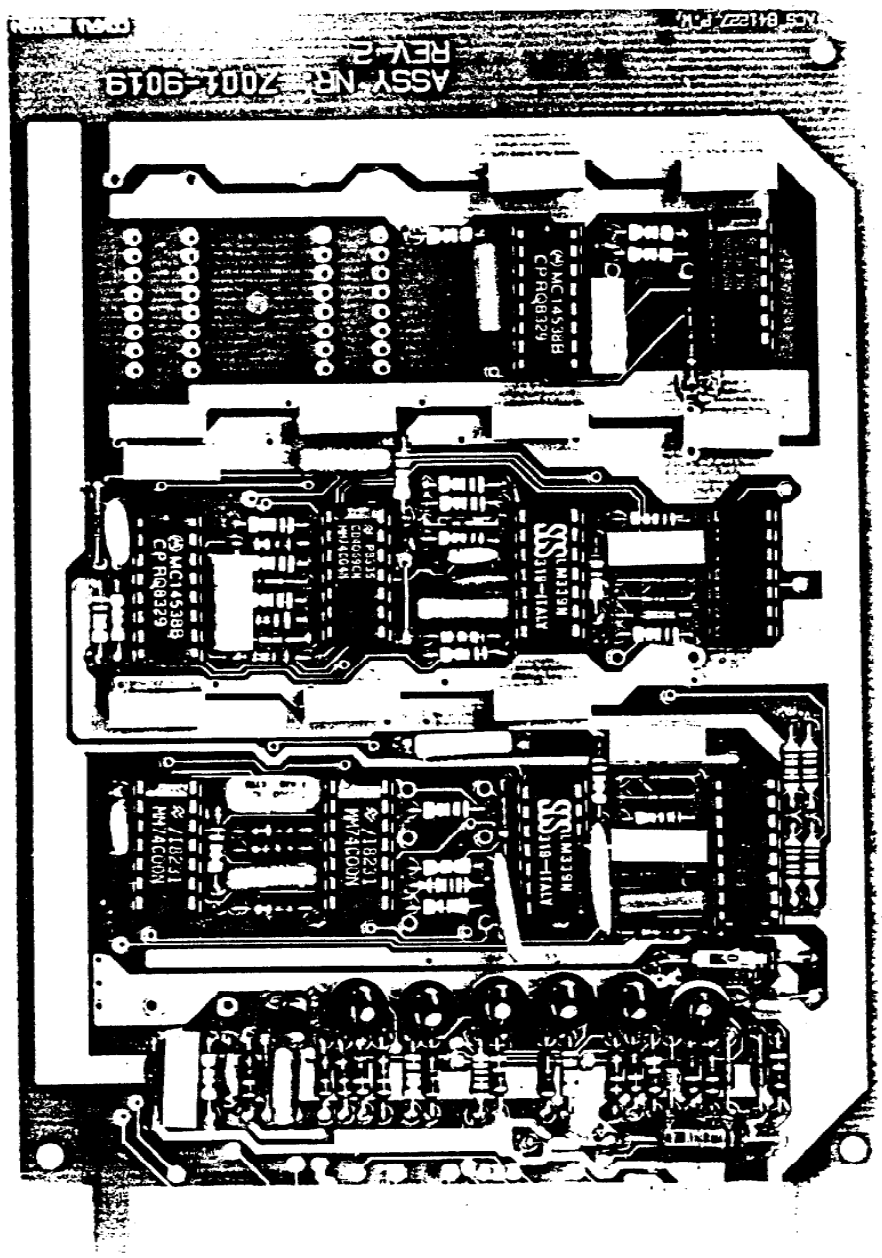
ANALOG BACKPLANE



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3.4.2

TRIGGER PRIMARY BD.(SLOT 12)



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A. TRIGGER PRIMARY BD. (SLOT 12)

THE TRIGGER PRIMARY BD IS RESPONSIBLE FOR PRODUCING THE FOLLOWING OUTPUTS:

1. CYL CLOCK
2. DELAYED DWELL
3. ENGINE SYNC
4. PRIM. AVAILABLE
5. SEC.AVAILABLE

1. CYL CLOCK

CYL CLOCK IS NORMALLY GENERATED FROM THE PRIMARY KL1 SIGNAL. THE VOLTAGE THRESHOLD AT WHICH CYL CLOCK PULSES ARE PRODUCED IS VARRIED BY THE COMPUTER ACCORDING TO THE TEST CONDITIONS.

THERE ARE THREE THRESHOLDS AS FOLLOWS:

TEST CONDITION	THRESHOLD ON	THRESHOLD OFF
A. NORMAL	80v	4v
B. ENGINE KILL/CYLINDER SHORT	12v	4v
c. IDLE MIXTURE CONTROL (KL1 CONNECTED TO CARBURETTOR)	4v	4v

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THESE THRESHOLDS ARE CONTROLLED BY SWITCHING FETS. THAT ADJUST A POTENTIAL DIVIDER. THE FET SWITCHES ARE IN TURN CONTROLLED BY THE 4VOLT AND CYL SHORT LINES. (SEE MISCELLANEOUS FUNCTION BD.)

DURING NORMAL OPERATION THE LEADING EDGE OF THE PRIMARY SIGNAL TRIGGERS THE CYL CLOCK GENERATOR AT 80v THEN AFTER A PRESET TIME THE THRESHOLD IS ADJUSTED VIA A FET. SWITCH TO 4 VOLTS FOR THE TRAILING EDGE OF THE PRIMARY PULSE.

DURING ENGINE KILL (CRANKING) OR CYLINDER SHORTING, CYL CLOCK IS STILL REQUIRED AND THEREFORE THE TRIGGER THRESHOLD MUST BE ADJUSTED. THIS IS ACHIEVED VIA THE CYL SHORT LINE WHICH IS CONTROLLED BY THE COMPUTER. THE CYL SHORT LINE MAY BE ACTIVE CONTINUOUSLY AS DURING ENGINE KILL OR MOMENTARILY TO CORRESPOND TO A PARTICULAR CYLINDER AS DURING CYLINDER SHORTING.
THE CYL SHORT LINE ACTIVATES ANOTHER FET SWITCH WHICH BRINGS THE LEADING EDGE THRESHOLD DOWN TO 12V, THE TRAILING EDGE REMAINS AT 4V.

DURING IDLE MIXTURE CONTROL MEASUREMENT THE THRESHOLD NEEDS TO BE FURTHER REDUCED TO 4V SO THAT THE TESTER NAY TRIGGER FROM THE SIGNAL GENERATED BY THE IDLE MIXTURE CONTROL UNIT. THIS IS ACHIEVED VIA THE 4VOLT LINE. THE 4VOLT LINE (CONTROLLED BY THE MISCELLANEOUS FUNCTION BD) GOES ACTIVE LOW WHEN N0 (0R A VERY LOW) SIGNAL IS DETECTED AT THE GREEN(KL1) CLIP. THE 4VOLT LI NE TH E N ACTIVATES A FET SWITCH FORCING THE LEADING EDGE THRESHOLD TO 4VOLTS THE TRAILING EDGE REMAINS AT 4VOLTS.

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CYLINDER CLOCK WILL BE GENERATED FROM THE SECONDARY (PATTERN P.U.) IF PRIMARY AVAILABLE AT PIN J Is Low (PRIMARY NOT CONNECTED).

CYLINDER CLOCK IS OUTPUTTED AT PIN R.
AN INVERTED CYLINDER CLOCK (CYL CLK) IS OUTPUTTED AT PINS 9 AND L.

CYL CLOCK AND CYL CLOCK ARE USED FOR VARIOUS FUNCTIONS WITHIN THE TESTER.

2. DELAYED DWELL

DELAYED DWELL IS USED BY THE COMPUTER TO DETERMINE THE DWELL ANGLE OF THE ENGINE UNDER TEST, AND IS GENERATED FROM THE PRIMARY (KL1) INPUT. TRIGGER THRESHOLD LEVELS ARE THE SAME AS FOR CYL CLK (SEE 1. CYL CLK). THE DELAYED DWELL MARK/SPACE RATIO IS PROPORTIONAL TO THE DWELL ANGLE. THE DWELL SIGNAL IS SLIGHTLY DELAYED DUE TO FILTERING IN THE OUTPUT, HENCE THE NAME DELAYED DWELL. DELAYED DWELL IS OUTPUTTED AT PIN 11.

AN INVERTED DELAYED DWELL (DEL.DWELL) IS OUTPUTTED AT PIN 12.

DELAYED DWELL IS ALSO FED TO THE MUX A/D TO INFORM THE TESTER WHEN TO MEASURE DISTRIBUTOR RESISTANCE. (SEE SECTION 5 MUX A/D).

NOTE:
DELAYED DWELL CAN ONLY BE GENERATED FROM PRIMARY (KL1).

THE DWELL CIRCUITRY CAN ALSO BE USED TO MONITOR THE IDLE MIXTURE CONTROL UNIT (OPTION).

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3. ENGINE SYNC

ENGINE SYNC IS USED BY THE TESTER TO DETERMINE NO.1. CYLINDER AND FOR GENERATION OF THE TIMING AND LITEFIRE PULSES ON THE TIMING BD. (SEE TIMING BD.)

ENGINE SYNC IS GENERATED FROM THE RED TRIGGER CLAMP. AS THE GENERATION OF SPURIOUS ENGINE SYNC PULSES DUE TO PICKUP FROM THE OTHER SPARK LEADS IS POSSIBLE IT IS NECESSARY TO FIRST FEED THE TRIGGER SIGNAL TO A COMPARATOR TO ENSURE ONLY SIGNALS GREATER THAN APPROX 150mV GENERATE ENGINE SYNC PULSES.

ENGINE SYNC IS OUTPUTTED AT PIN 14.

4. PRIMARY AVAILABLE.

PRIMARY AVAILABLE IS USED TO INFORM THE COMPUTER AS TO WHETHER OR NOT THE PRIMARY LEAD IS CONNECTED. THIS SIGNAL IS A DC LEVEL AND IS ACTIVE HIGH.

PRIMARY AVAILABLE IS OUTPUTTED AT PIN 13.

5. SECONDARY AVAILABLE.

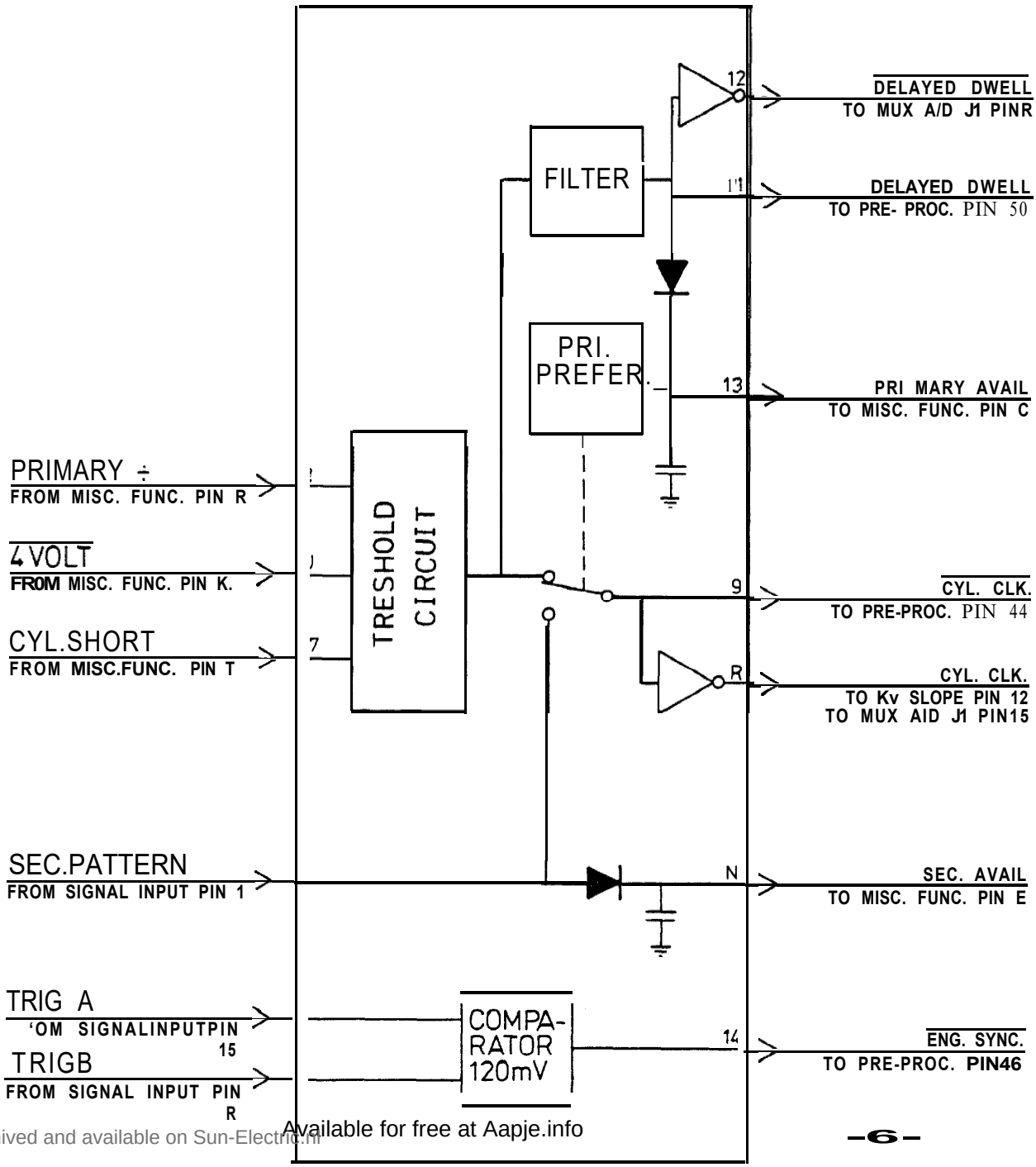
SECONDARY AVAILABLE IS USED TO INFORM THE COMPUTER AS TO WHETHER OR NOT THE SECONDARY (CHROME CLAMP) Is CONNECTED. THIS SIGNAL Is A DC. LEVEL AND IS ACTIVE HIGH.

SECONDARY AVAILABLE IS OUTPUTTED AT PIN N.

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TRIGGER PRIMARY BOARD

BLOCK DIAGRAM



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waveforms

NOTE: THE FOLLOWING WAVEFORMS ARE PRODUCED BY THE TESTER WHEN IT IS CONNECTED TO AN IS100A. THE SETTINGS OF THE IS100A AND THE TESTER MUST BE AS FOLLOWS:

IS100A

CONNECT- PRIMARY KL1
PRIMARY KL15
SECONDARY PATTERN
RED TRIGGER
ENGINE GROUND
BATT+

SETTINGS	CYLINDERS	4
	RPM	1000
	ALT/VOLT/OHMS	+12V
	POWER	ON
	IGNITION	ON
	ALL ELSE	OFF

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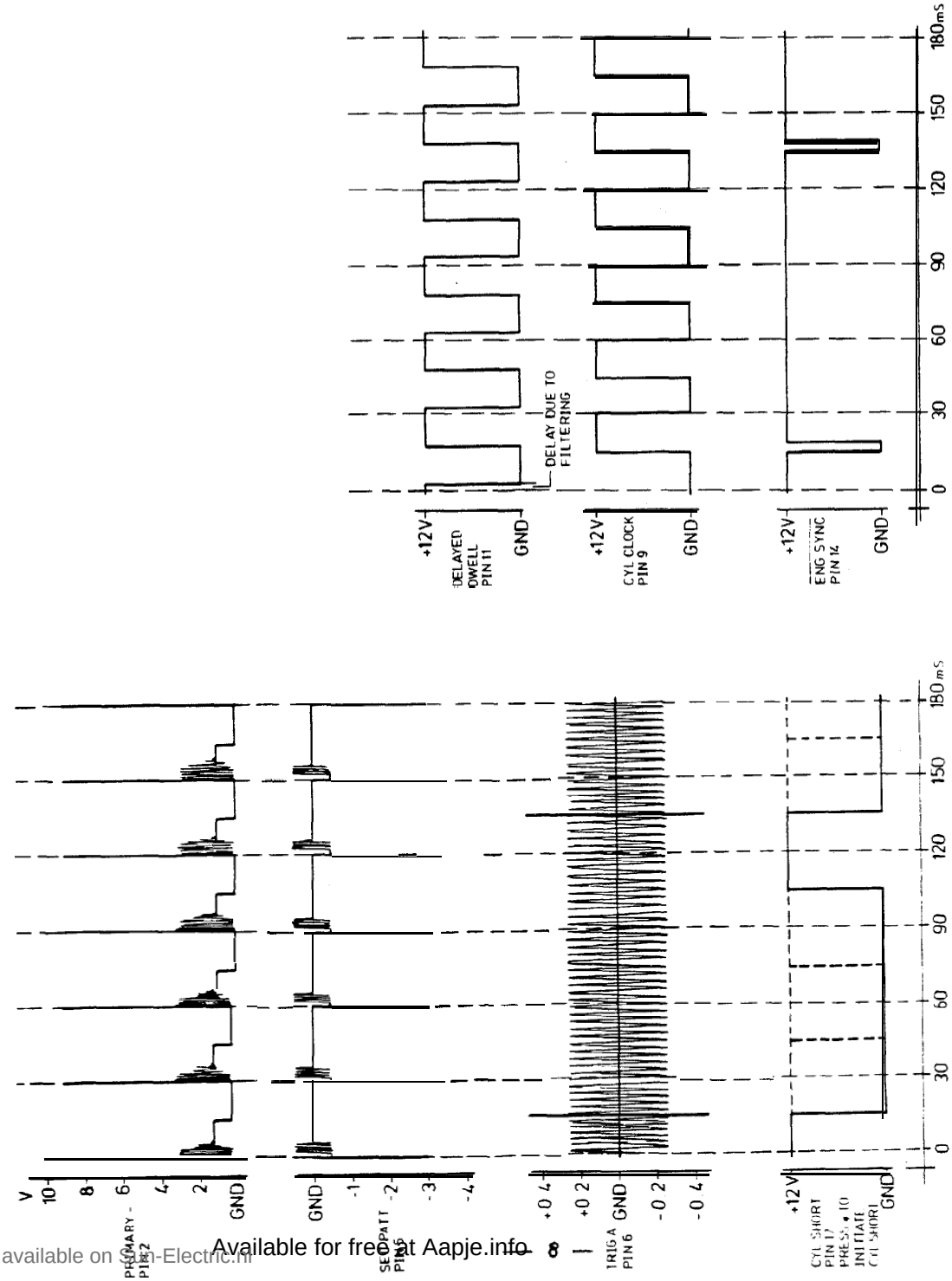
ALLOW SELF CALIBRATION

GO TO WORKSHOP TEST: SET NO.CYL TO 4

GO TO TEST 8 CYLINDER COMPARISON

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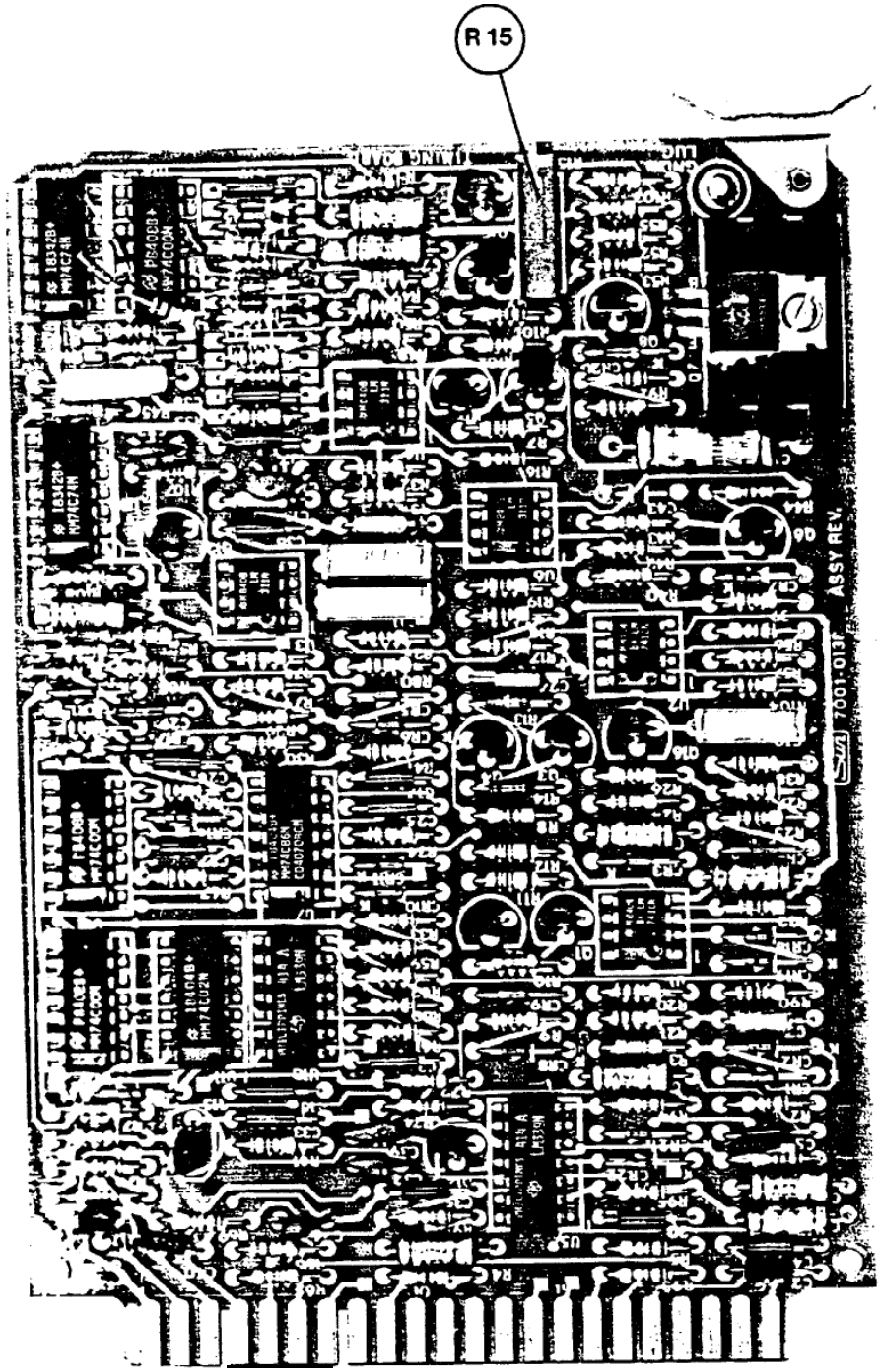
TRIGGER PRIMARY BD WAVEFORMS



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3.4.3

TIMING BOARD (SLOT 7)



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B. TIMING BOARD (SLOT 7)

THE TIMING BOARD IS RESPONSIBLE FOR PRODUCING THE TIMING PULSE. THIS CAN BE DONE FROM A VARIETY OF SOURCES:

1. EURO MAG.

2. DOM MAG.

3. TIMING LIGHT.

1. EURO MAG.

THE EURO MAG SIGNAL IS DETECTED BY INSERTING A TDC SENSOR (INDUCTIVE COIL) INTO THE ENGINE UNDER TEST. THIS COIL IS POWERED FROM A VARIABLE CURRENT SOURCE WHICH SETS UP A MAGNETIC FLUX, WHEN EITHER A PIN OR HOLE PASSES THROUGH THIS FLUX IT PRODUCES A PULSE ON THE LINE. AS THE AMPLITUDE OF THIS PULSE IS DEPENDANT UPON THE DISTANCE BETWEEN THE PIN/HOLE AND THE ENGINE SPEED IT IS NECESSARY TO VARY THE CURRENT SOURCE TO MAINTAIN A STABLE AMPLITUDE. THIS IS DONE BY MONITORING THE RESULTANT PULSE AND USING THIS TO CONTROL THE CURRENT SOURCE, THUS PROVIDING AN AGC CIRCUIT. THE PULSE IS THEN PASSED TO A NOISE REJECTION/SHAPER CIRUIT AND A ZERO CROSSING DETECTOR.

THE TWO SIGNALS ARE FED TO A MONO STABLE TO PRODUCE THE RESULTANT TIMING PULSE. THIS IS OUTPUTTED VIA THE TIMING SELECT LOGIC AS THE PREFERRED SIGNAL. WHILST PRODUCING TIMING PULSES FROM EURO MAG, A MON LEVEL IS GENERATED.

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THIS HAS TWO FUNCTIONS:

1. IT TELLS THE COMPUTER THAT THE TESTER IS IN THE MAGNETIC MODE.
2. SWITCHES THE TIMING LIGHT TO 0^0 AND INHIBITS LITEFIRE TO AVOID TIMING INTERFERENCE.

2. DOM MAG (NOT USED)

3. TIMING LIGHT

TO MEASURE THE TIMING WITH THE TIMING LIGHT IT IS NECESSARY TO DELAY THE TIMING PULSE WITH RESPECT TO $\overline{\text{ENG SYNC}}$. THE LITEFIRE PULSE WHICH CAUSES THE TIMING LIGHT TO FLASH MUST ALSO BE DELAYED BY THE SAME AMOUNT. THE AMOUNT OF DELAY IS CONTROLLED BY THE POTENTIOMETER ON THE REAR OF THE TIMING LIGHT. THE 0^0 SWITCH (POT FULLY CCW) CAUSES THE DELAY TO BE SET TO ZERO. R15 SETS THE MAXIMUM TIMING READING TO 90^0 (SEE CAL PROCEDURE SEE SECTION 1.)

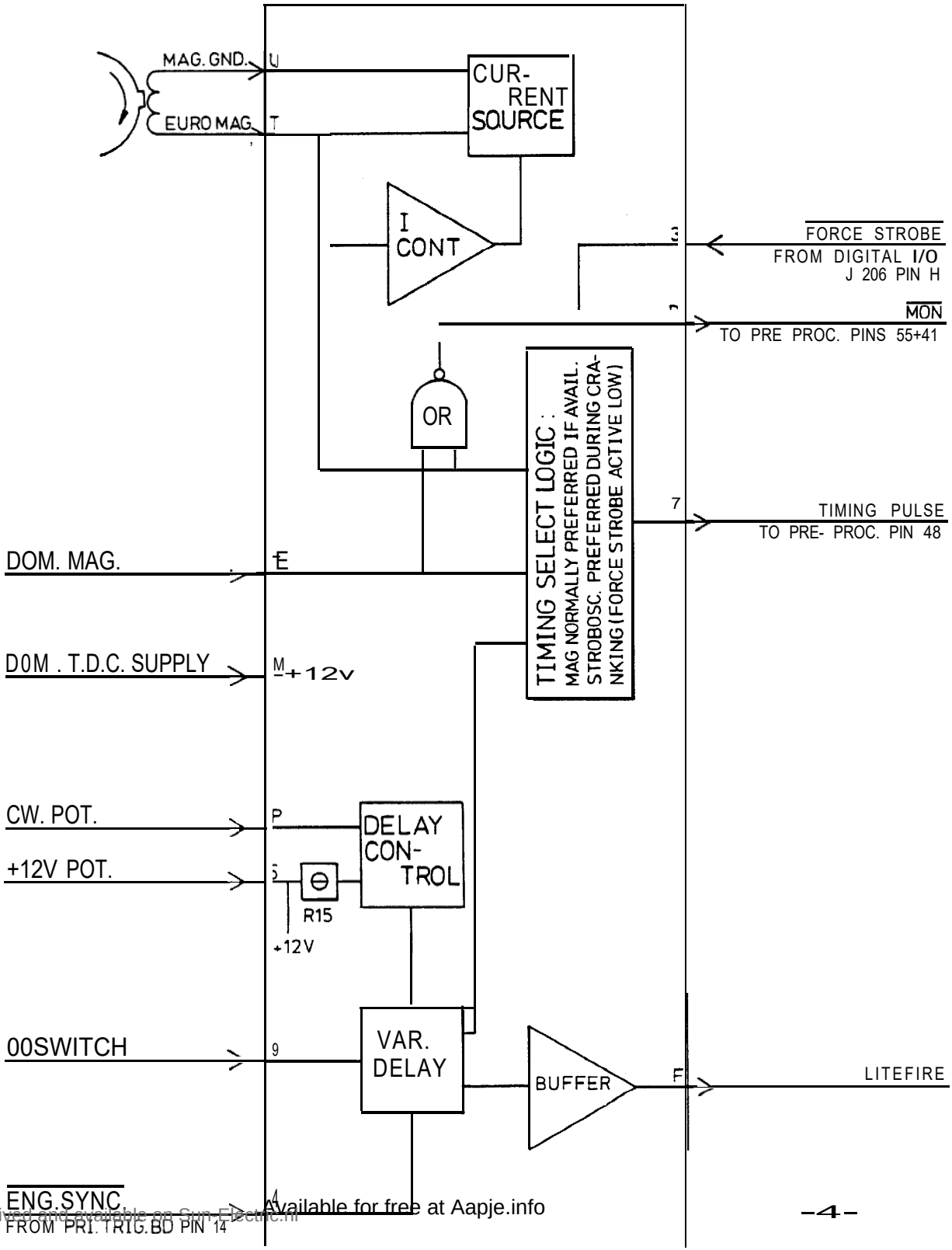
THE HOLD BUTTON ON THE TIMING LIGHT DOES NOT PASS THROUGH THE TIMING BD BUT IS FED DIRECTLY TO THE DIGITAL I/O TO FREEZE THE TIMING INFORMATION (SEE SECTION 5 DIGITAL I/O).

$\overline{\text{FORCE STROBE}}$ IS GENERATED BY THE COMPUTER DURING CRANKING, CAUSING THE TIMING SELECT LOGIC TO PREFER STROBOSCOPIC TIMING EVEN THOUGH EURO MAG IS AVAILABLE. THIS IS DUE TO MAG SIGNAL BEING INHERENTLY UNRELIABLE AT LOW R.P.M.

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BLOCKDIAGRAM

TIMING BD



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WAVEFORMS

NOTE: THE FOLLOWING WAVEFORMS ARE PRODUCED BY THE TESTER WHEN IT IS CONNECTED TO AN IS100A. THE SETTINGS OF THE IS100A AND THE TESTER MUST BE AS FOLLOWS:

Is100A

CONNECT-	PRIMARY KL1	
	PRIMARY KL15	
	SECONDARY PATTERN	
	RED TRIGGER	
	ENGINE GROUND	
	BATT+	
SETTINGS	CYLINDERS	4
	RPM	1000
	ALT/VOLT/OHMS	+12V
	POWER	ON
	IGNITION	ON
	ALL ELSE	OFF

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ALLOW SELF CALIBRATION

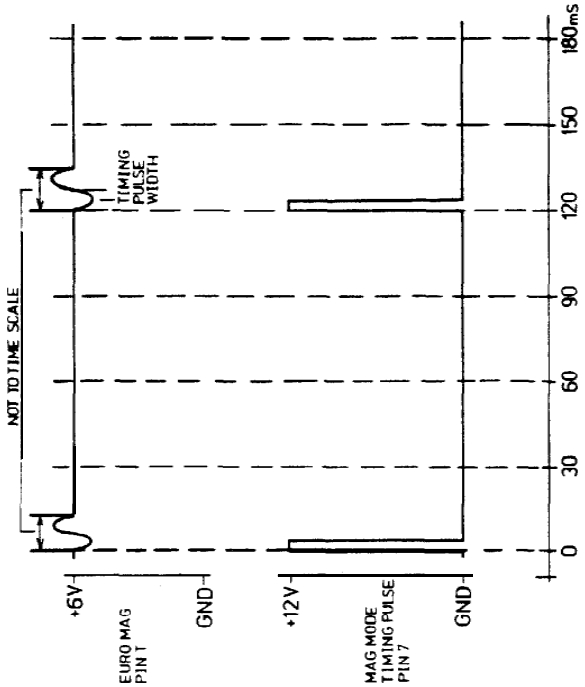
GO TO WORKSHOP TEST: SET NO.CYL TO 4

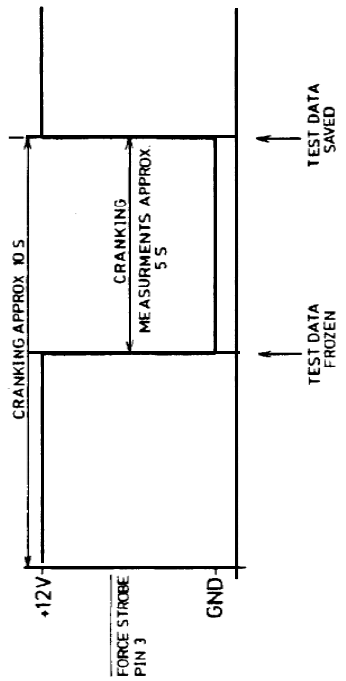
GO TO TEST 14 IGNITION WITHOUT VACUUM.

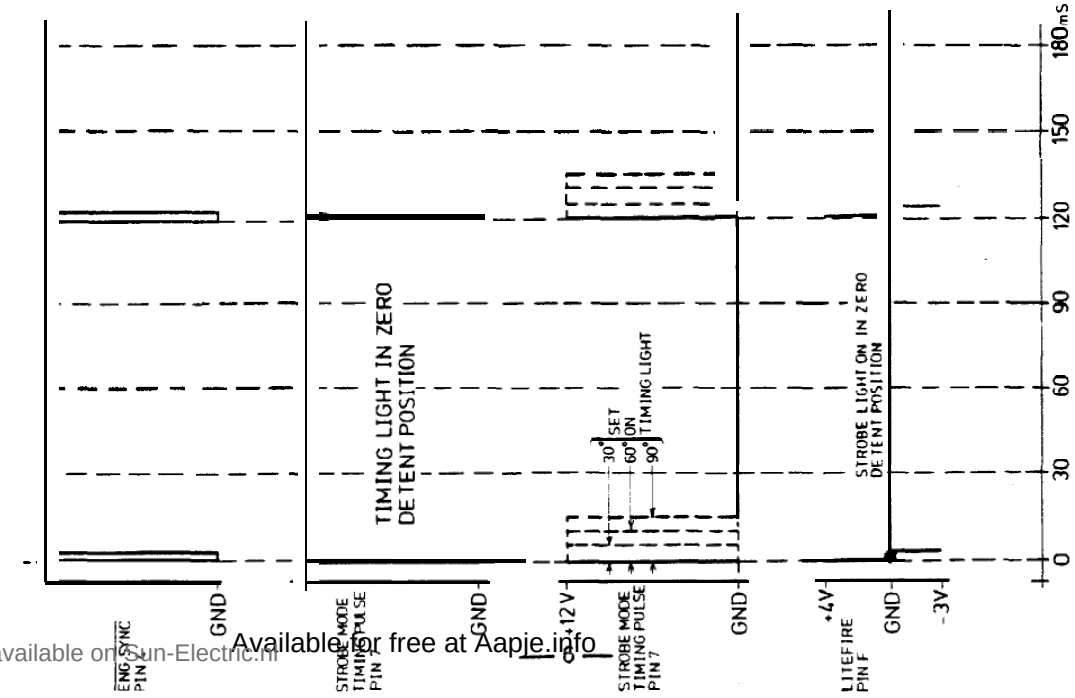
WHEN REQUIRED USE MAG PROBE 018-206N.

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TIMING BD WAVEFORMS



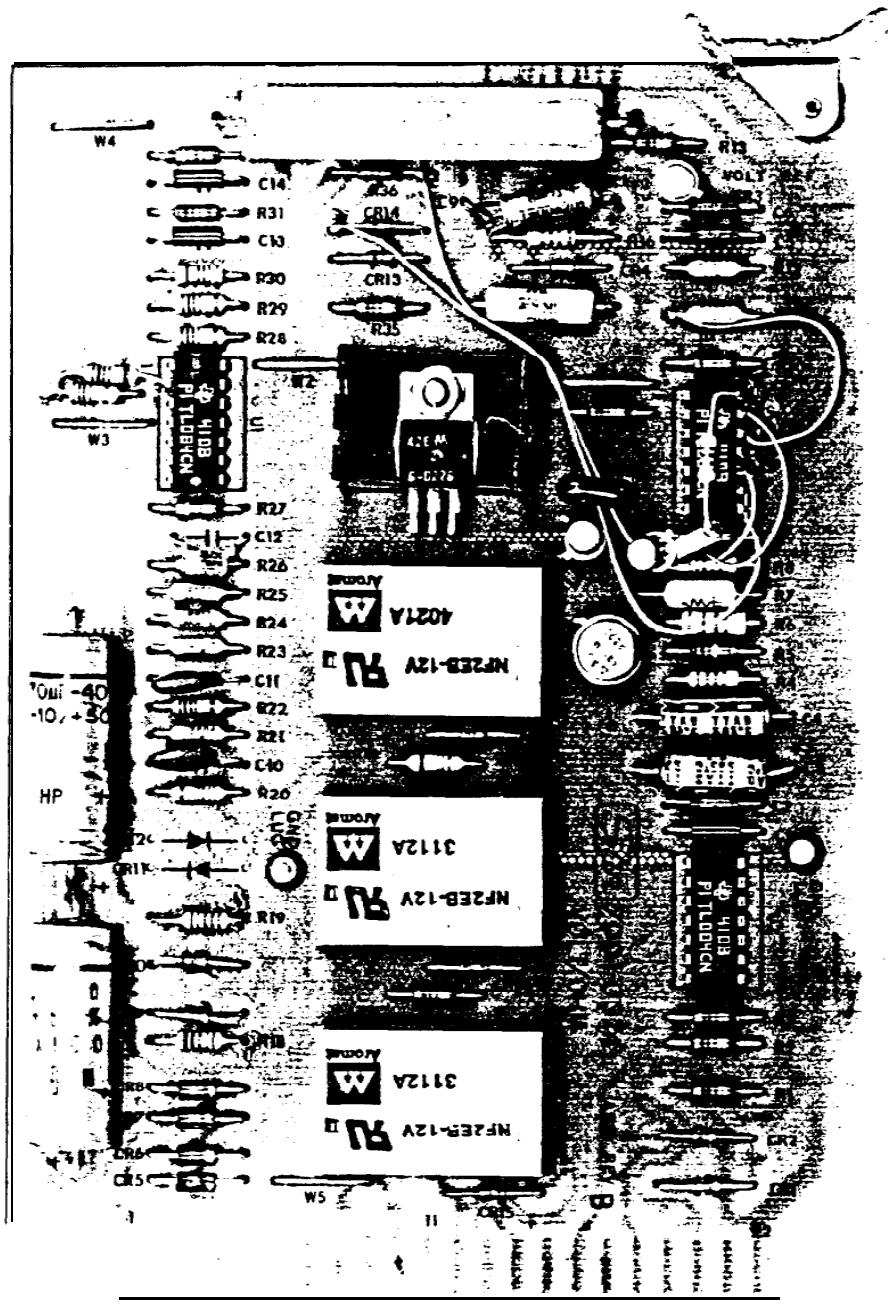




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3,4,4

VOLT/OHM BD (SLOT 5)



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C. VOLT/OHM BD (SLOT 5)

THE VOLT/OHM BOARD ALLOWS THE OPERATOR TO MAKE PIN POINT VOLTAGE , AND CONTINUITY MEASUREMENTS. THIS FACILITY IS ONLY AVAILABLE ON THE SECOND MULTIMETER PAGE (SEE FLOW DIAGRAM PAGE 4 + 5 INTRODUCTION) AND IS DISPLAYED DIGITALY AND AS A BAR GRAPH.
THE VOLT/OHM PROBES ARE FULLY ISOLATED FROM THE REST OF THE TESTER TO PROTECT AGAINST SHORT CIRCUITS. THIS IS ACHEIVED BY INCORPERATING AN ISOLATED POWER SUPPLY OF +/- 10V.

THE VOLT/OHM BOARDS OUTPUT VOLT/OHM ANA IS FED DIRECTLY TO THE MUX A/D FOR MEASUREMENT BY THE COMPUTER. THE COMPUTER ALSO HAS CONTROL OVER THE VOLT/OHM BD VIA TWO CONTROL LINES:

1. $\overline{\text{VOLTS}}$. THIS LINE SWITCHES BETWEEN VOLTS AND OHMS.

   NOTE: IT IS ONLY POSSIBLE TO ENTER THE OHMS MODE IF THE VOLT/OHMS LEADS ARE SHORTED TOGETEHER.

2. $\overline{\text{OHM X 1K}}$. THIS LINE WHEN IN THE OHMS RANGE SWITCHES TO A X 1000 RANGE.

   NOTE: OHMS ARE FULLY AUTORANGING, HOWEVER THE SOFTWARE ENABLES THE OPERATOR TO FREEZE ON ANY DESIRED RANGE BY DEPRESSING THE * BUTTON
   THESE RANGES ARE AS FOLLOWS:

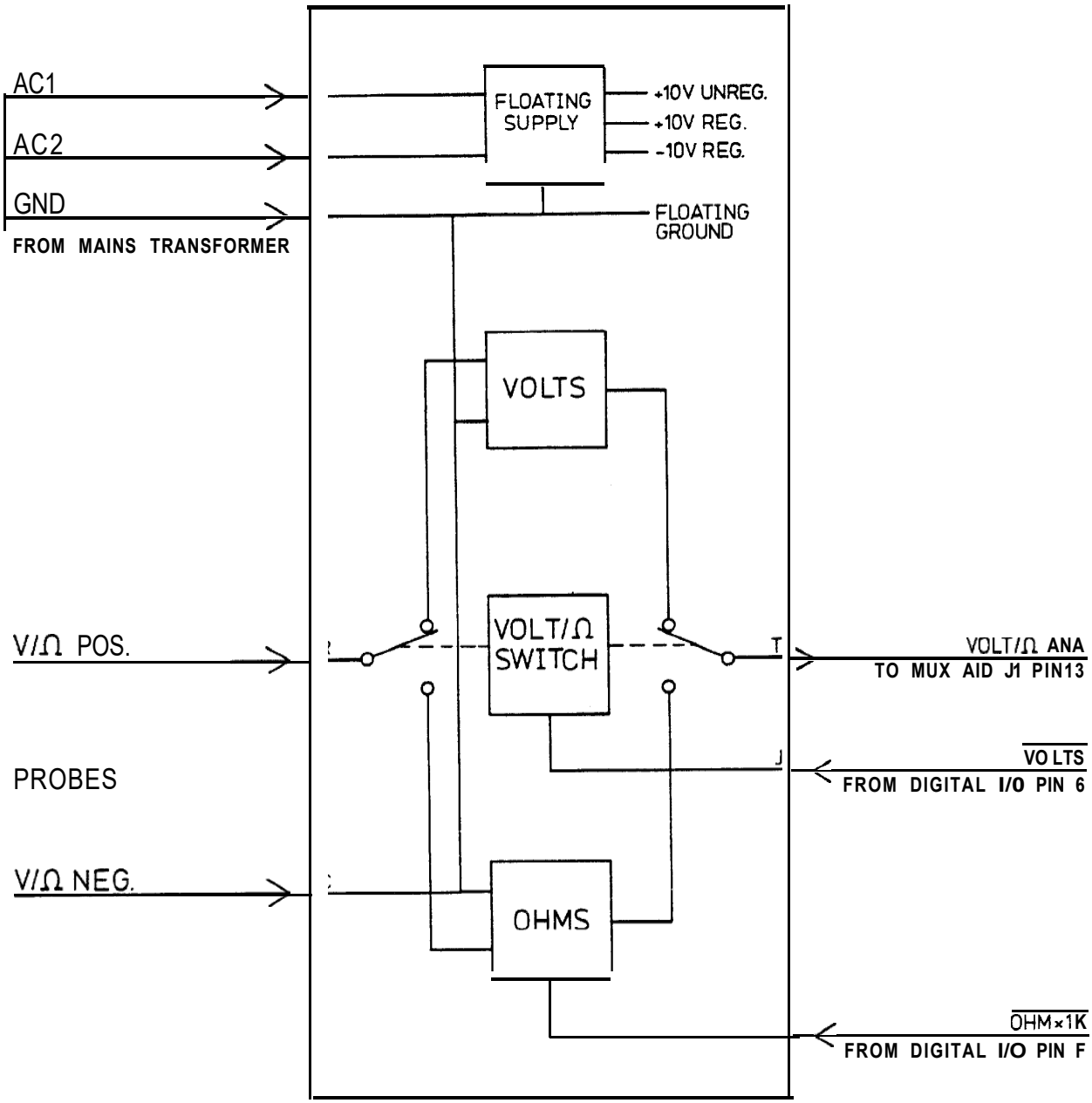
   0-1 Ω x l X10 X100 X1K X10K X100K
   0-2,5 Ω Xl X10 X100 X1K X10K X100K
   0-5 Ω x l X10 X100 X1K X10K

   (SEE OPERATING INSTRUCTIONS INTRODUCTION).

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VOLT/OHM BOARD

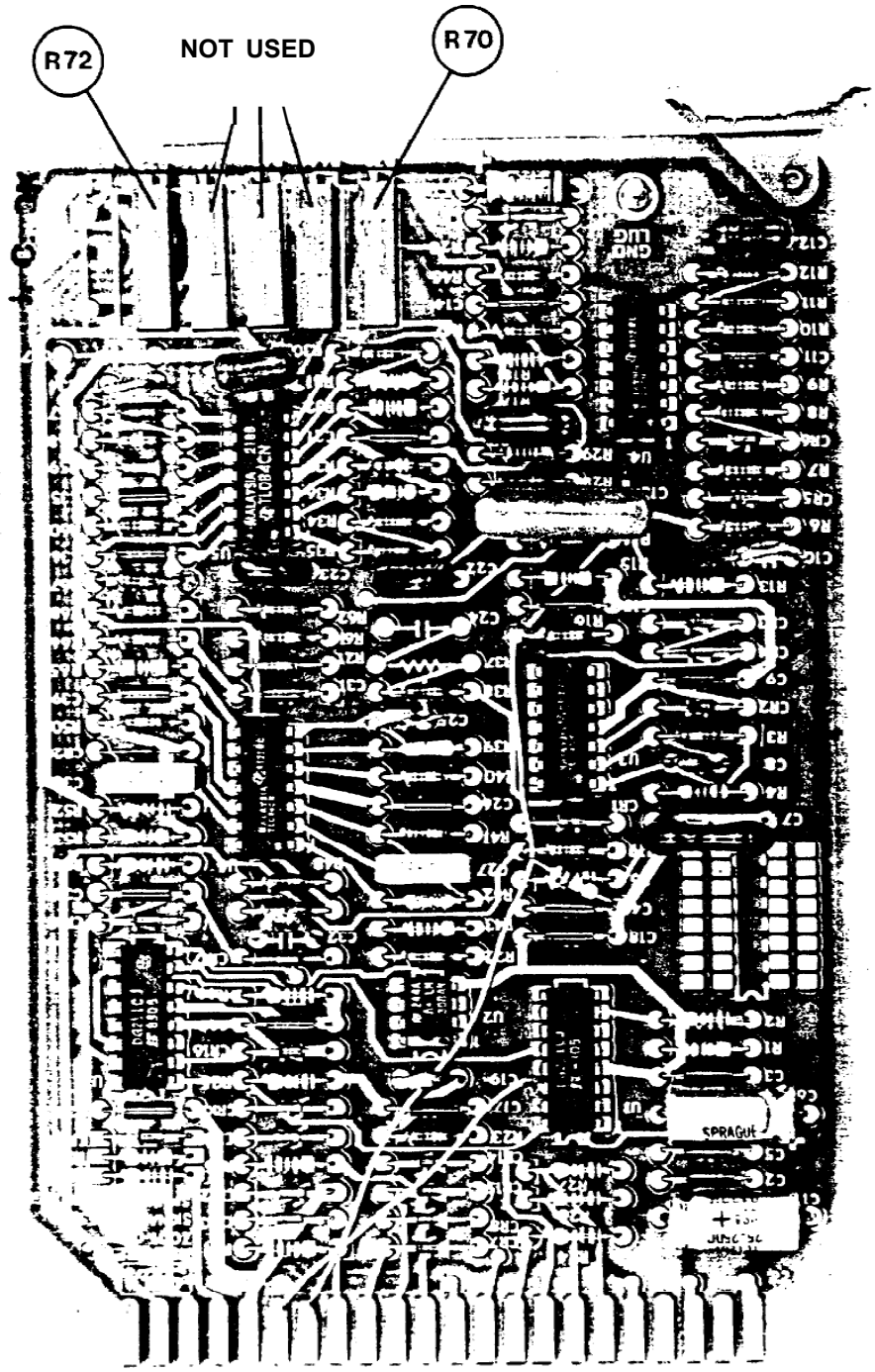
BLOCK DIAGRAM



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3.4.5

KV PROCESSOR BD (SLOT 4)



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D. K.V PROCESSOR BOARD (SLOT 4)

THE K.V. PROCESSOR BOARD IS USED FOR TWO MAIN TASKS:

1. TO SAMPLE THE PATTERN INPUT AND MAKE IT SUITABLE FOR READING BY THE COMPUTER VIA THE MUX A/D.
   A SWITCHED PATTERN OUTPUT IS ALSO MADE AVAILABLE FOR THE KV SLOPE BD (SEE SECTION 4 KV SLOPE BD).
2. TO PROVIDE BATT RIPPLE ANA TO BE USED BY THE MUX A/D FOR DISPLAY.

1. THE PEAK KV. ANA OUTPUT IS DEVELOPED BY CHARGING A CAPACITOR TO THE PEAK VALUE OF THE PATTERN PULSE, AND DISCHARGING IT AFTER EACH PATTERN PULSE. THIS IS ACHEIVED BY USING THE COMPUTER TO CONTROL THE KV. PROCESSOR VIA THE KV. CARD READER (SEE SECTION 5). THE CONTROL FUNCTIONS ARE AS FOLLOWS:

$\overline{\text{READ}}$: NOT USED (PERMANENTLY Low ACTIVE)

$\pm$ PEAK SELECT: AT PRESENT NOT USED BY SOFTWARE REV 1.0. COULD BE USED LATER FOR CALIBRATION.

RING CNT: GENERATED BY THE KV. PROCESSOR TO INFORM THE COMPUTER THAT THE SPARK DURATION IS COMPLETE AND IS READY FOR READING AND DISPLAY.

DISCHARGE: RESETS CIRCUITS TO ZERO READY FOR NEXT SAMPLE.

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TEST: FOR ZERO CALIBRATION OF PEAK AND SPARK KV.'S DURING CALIBRATION PERIOD.

2. THE BATTERY RIPPLE SIGNAL FROM THE SIGNAL INPUT BD IS FILTERED AND BUFFERED AND FED TO THE MUX A/D WHERE THE COMPUTER READS AND DISPLAYS IT AS A PERCENTAGE OF BATTERY VOLTS.

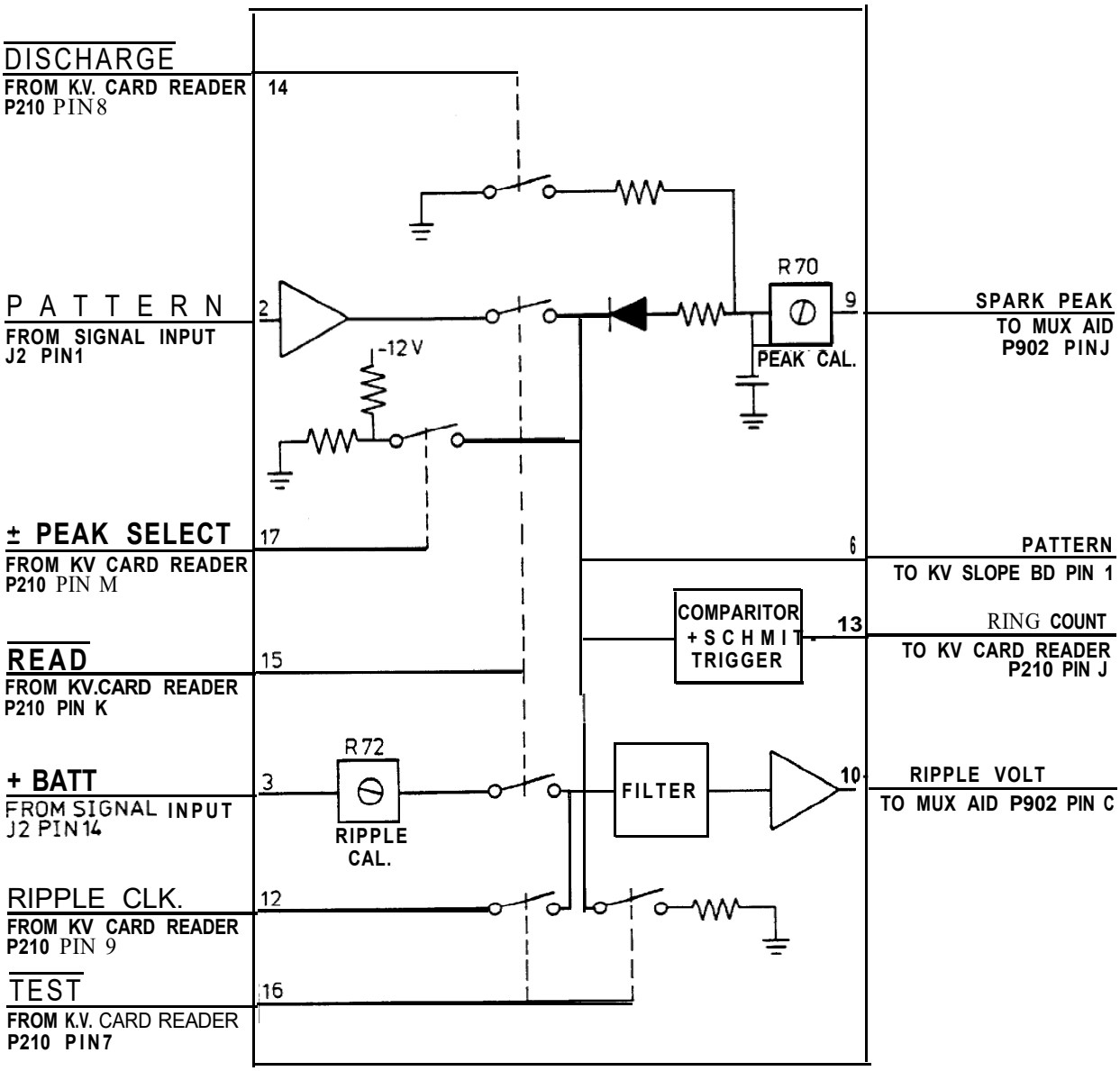
DURING THE CALIBRATION PERIOD TEST IS ACTIVATED AND A SIMULATED RIPPLE IS APPLIED TO THE RIPPLE CHK INPUT. THIS ALLOWS THE COMPUTER TO CALIBRATE THE BATT. RIPPLE CIRCUIT.

NOTE: NOT USED WITH SOFTWARE REVISION 1.0. SEE SECTION 11.

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K.V. PROCESSOR BD

BLOCK DIAGRAM



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WAVEFORMS

NOTE: THE FOLLOWING WAVEFORMS ARE PRODUCED BY THE TESTER WHEN IT IS CONNECTED TO AN IS100A. THE SETTINGS OF THE IS100A AND THE TESTER MUST BE AS FOLLOWS:

IS100A

CONNECT- PRIMARY KL1

PRIMARY KL15

SECONDARY PATTERN

RED TRIGGER

ENGINE GROUND

BATT+

SETTINGS	CYLINDERS	4
	RPM	1000
	ALT/VOLT/OHMS	+12V
	POWER	ON
	IGNITION	ON
	ALL ELSE	OFF

SUN-2014

ALLOW SELF CALIBRATION

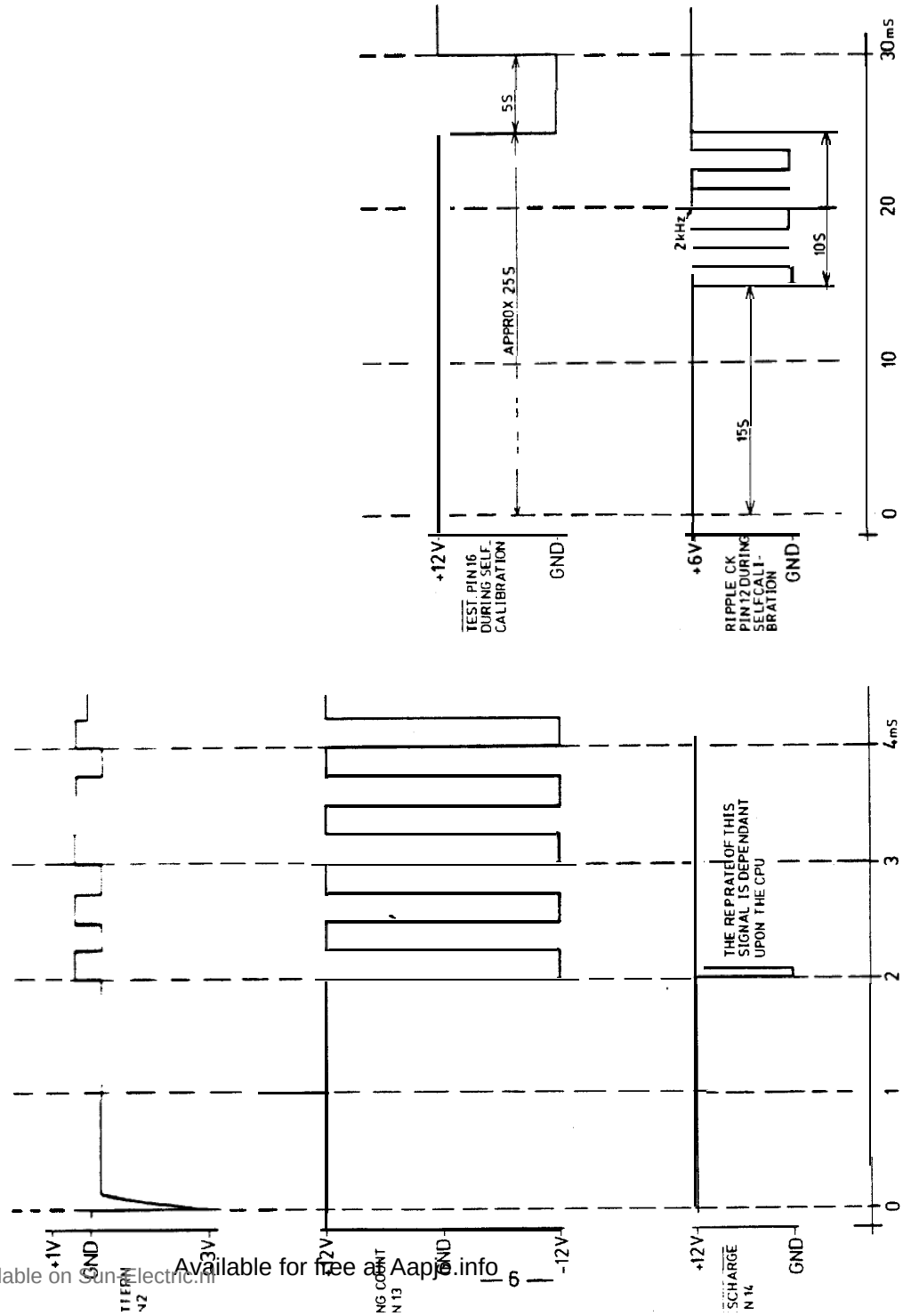
GO TO WORKSHOP TEST: SET NO.CYL TO 4

GO TO TEST 6 IGNITION SECONDARY.

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K.V. PROCESSCR BD

WAVEFOFMS



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K.V. PROCESSOR BD.

GENERAL

THE OUTPUT STAGE OF THE BATTERY RIPPLE CIRCUIT HAS BEEN MODIFIED TO GIVE A BETTER REPRESENTATION OF PEAK TO PEAK RIPPLE.
THIS IS ACHIEVED BY FEEDING THE AC RIPPLE SIGNAL TO A NEGATIVE AND POSITIVE PEAK DETECTING CIRCUIT AND COMPARING THE LEVELS. THUS THE DC OUTPUT IS DIRECTLY PROPORTIONAL TO THE PEAK TO PEAK VALUE.

IMPORTANT

MODIFIED AND UNMODIFIED BOARDS ARE FULLY INTERCHANGEABLE.

CALIBRATION

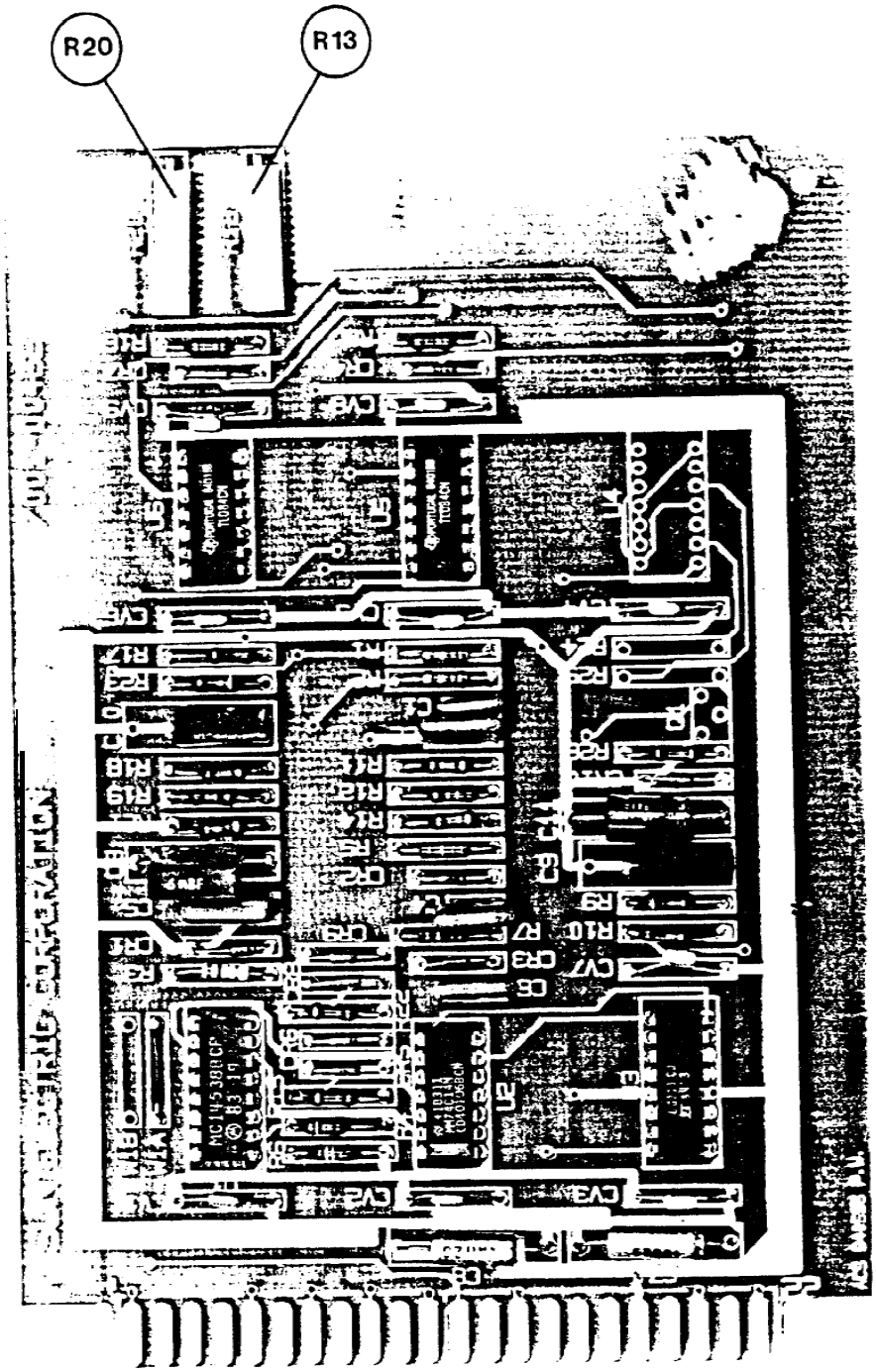
DUE TO THE CHANGE IN MEASURING TECHNIQUES IT IS ALSO NECESSARY TO CHANGE THE CALIBRATION VALUE.
THE CALIBRATION PROCEDURE AS DESCRIBED IN THE SERVICE REPAIR MANUAL STILL APPLIES, HOWEVER THE 10.2 % ALT. RIPPLE CALIBRATION VALUE REFERRED TO IN SECTION 1 PAGE 17 SHOULD NOW READ 11.5 %.

THIS NEW VALUE CORRESPONDS TO 1.5V PEAK TO PEAK RIPPLE SIGNAL SUPERIMPOSED UPON A 13V DC BATTERY LEVEL.

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3.4.6

K.V. SLOPE BD. (SLOT 2)



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E. K.V. SLOPE BD. (SLOT 2)

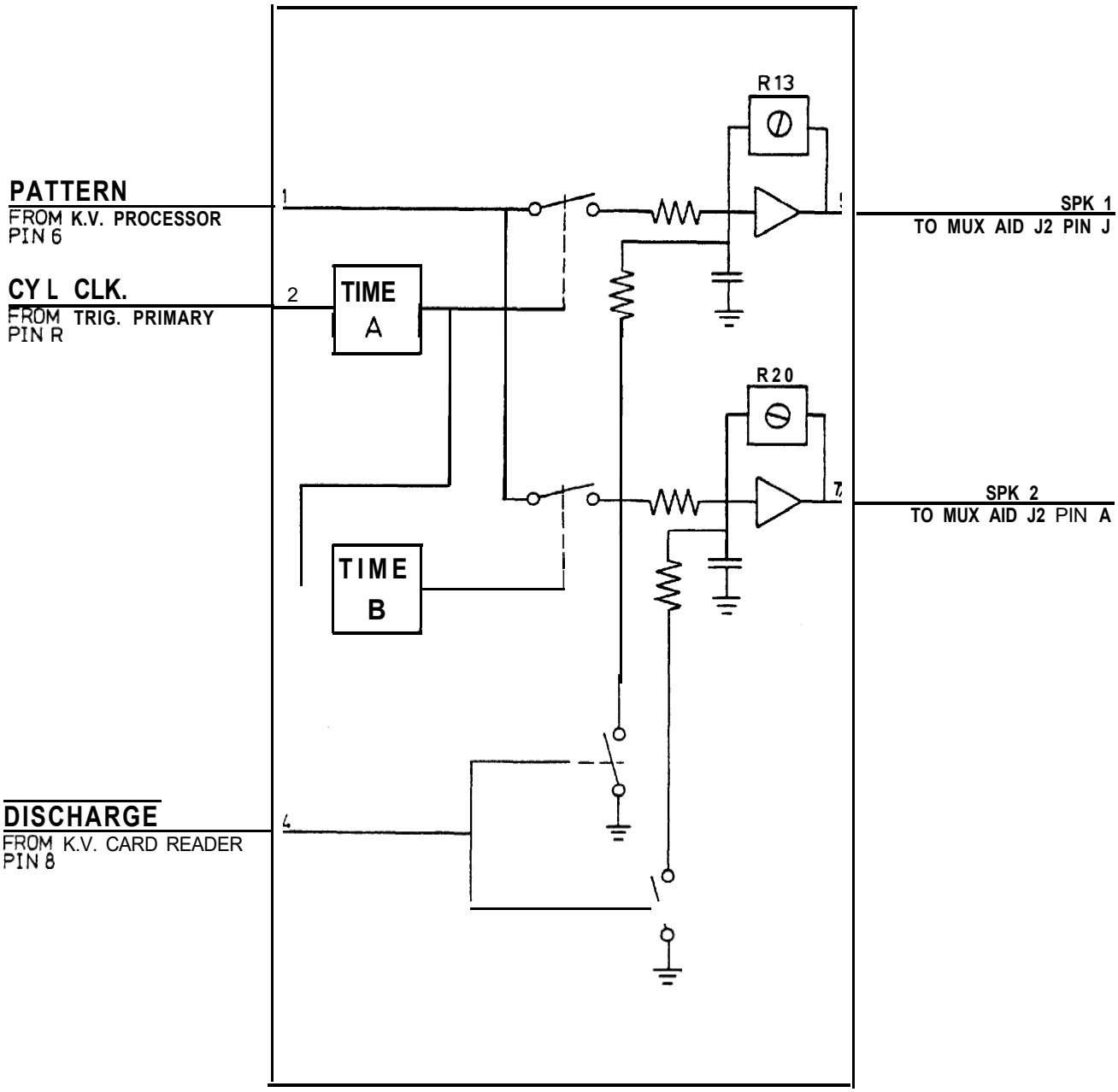
THE K.V. SLOPE BD. PRODUCES TWO ANALOG OUTPUTS THAT CORRESPOND TO TWO SAMPLE MEASUREMENTS MADE ALONG THE SPARK LINE OF EACH CYLINDER.
THIS IS ACHIEVED BY TWO CASCADED TIMERS THAT SWITCH THE PATTERN INPUT TO TWO STORAGE CAPACITORS AT PRE-DETERMINED SAMPLE PERIODS. THE CYL CLOCK SIGNAL IS USED TO TRIGGER THE TIMERS AND AT THE END OF EACH FIRING LINE THE DISCHARGE SIGNAL DISCHARGES THE CAPACITORS TO GROUND.

THE REVISION 1.0 SOFTWARE ONLY MAKES USE OF SPK2 WHICH IS DISPLAYED AS SPARK VOLTAGE.

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K.V. SLOPE BD

BLOCK DIAGRAM



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WAVEFORMS

NOTE: THE FOLLOWING WAVEFORMS ARE PRODUCED BY THE TESTER WHEN IT IS CONNECTED TO AN IS100A. THE SETTINGS OF THE IS100A AND THE TESTER MUST BE AS FOLLOWS:

IS100A

CONNECT- PRIMARY KL1

PRIMARY KL15

SECONDARY PATTERN

RED TRIGGER

ENGINE GROUND

BATT+

SETTINGS	CYLINDERS	4
	RPM	1000
	ALT/VOLT/OHMS	+12V
	POWER	ON
	IGNITION	ON
	ALL ELSE	OFF

MCS -2000

ALLOW SELF CALIBRATION

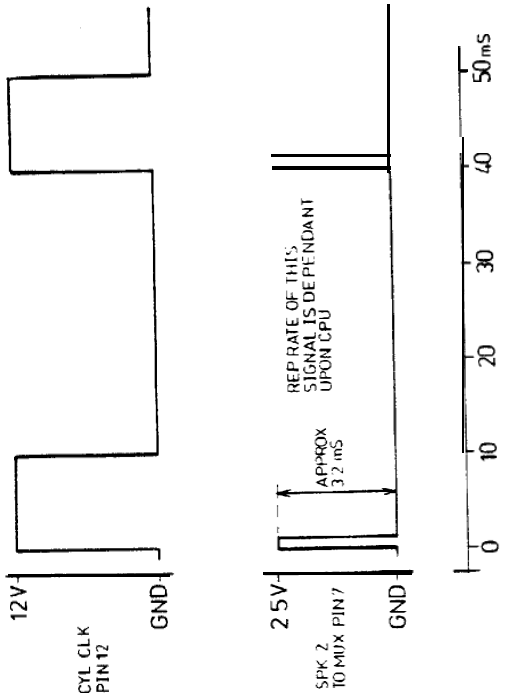
GO TO WORKSHOP TEST: SET NO.CYL TO 4

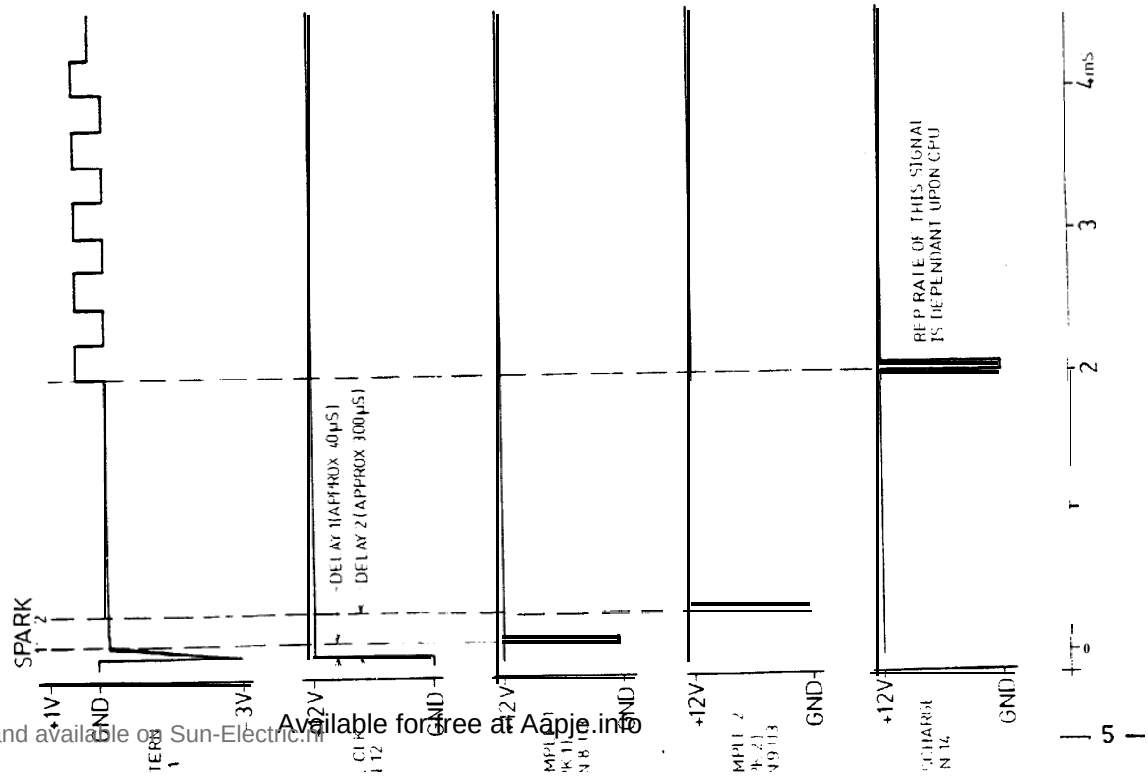
GO TO TEST 6 IGNITION SECONDARY.

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KV SLOPE BD

WAVEFORMS

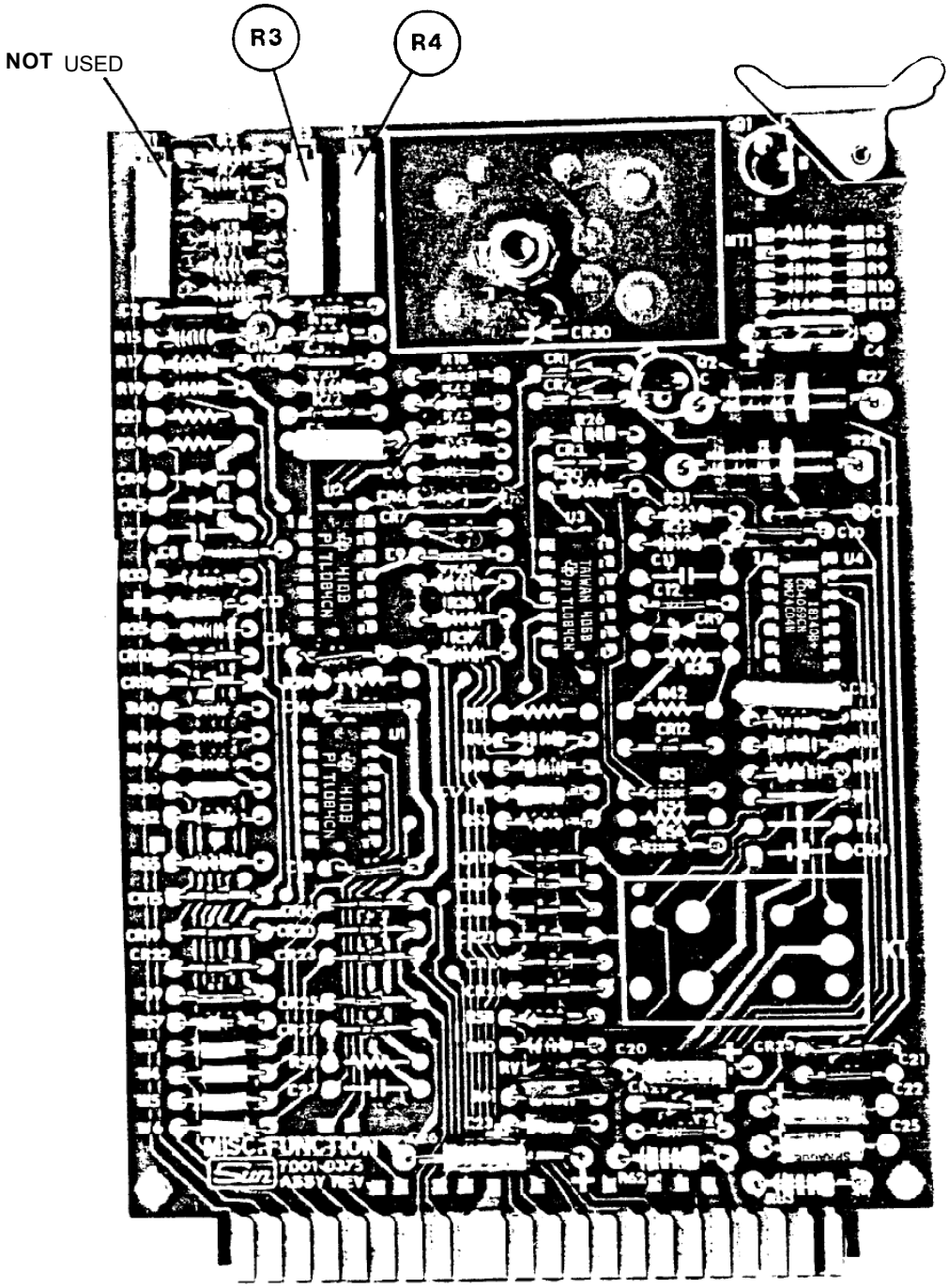




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3.4.7

MISCELLANEOUS FUNCTION BD. (SLOT 11)



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F. MISCELLANEOUS FUNCTION BD (SLOT 11)

THE MISCELLANEOUS FUNCTION BD PERFORMS A VARIETY OF TASKS WITHIN THE TESTER, THESE HAVE BEEN BROKEN DOWN AS FOLLOWS:

(A) PRODUCING SHORT

(B) PRODUCING 4VOLT

(c) BUFFERING SECONDARY AVAILABLE

(D) LIMITING PRIMARY AVAILABLE

(E) PRODUCING VAC ANALOG

(A) SHORT

THE SHORT LINE IS USED BY THE SIGNAL INPUT BD TO INITIATE A SHORT ACROSS THE PRIMARY OF THE ENGINE UNDERTEST.(SEE SIGNAL INPUT BD SECTION 3.)
THE SHORT LINE IS CONTROLLED BY ONE OF TWO SIGNALS FROM THE COMPUTER:

ENGINE KILL. THIS SIGNAL IS TAKEN FROM THE DIGITAL I/O, AND IS ACTIVE LOW DURING A CRANKING TEST OR WHEN MANUALY SET VIA THE REMOTE CONTROL.

SELECTED CYLINDER. THIS SIGNAL IS TAKEN FROM THE PRE-PROCESSOR AND IS ACTIVATED BY THE COMPUTER TO CORRESPOND TO A PARTICULAR CYLINDER DURING CYLINDER ANALYSIS TESTS.

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DURING EITHER ENGINE KILL OR CYLINDER SHORTING THE CYL SHORT LINE BECOMES ACTIVE TO REDUCE THE TRIGGER THRESHOLD OF THE TRIGGER PRIMARY BD SO AVOIDING MISTRIGGERING (SEE TRIGGER PRIMARY BD).

WHEN THE CYL SHORT LINE IS ACTIVE THE THRESHOLD AT WHICH THE $\overline{\text{4VOLT}}$ LINE BECOMES ACTIVE IS REDUCED TO APPROX 8V.

(B) $\overline{\text{4VOLT}}$.

DURING NORMAL RUNNING ENGINE CONDITIONS THE $\overline{\text{4VOLT}}$ LINE BECOMES ACTIVE WHEN A SIGNAL BELOW APPROX 30V IS DETECTED AT THE PRIMARY INPUT. WHEN THIS OCCURS, THE TRIGGER PRIMARY BD IS FORCED TO LOWER ITS TRIGGERING THRESHOLDS TO APPROXIAMATELY 4VOLT, THUS ALLOWING THE MEASUREMENT OF IDLE MIXTURE CONTROL UNITS (SEE TRIGGER PRIMARY BD). DURING ENGINE KILL OR CYLINDER SHORTING THE THRESHOLD, AT WHICH THE $\overline{\text{4VOLT}}$ LINE BECOMES ACTIVE, IS REDUCED TO APPROX 8v. THIS PREVENTS THE $\overline{\text{4VOLT}}$ LINE BECOMING ACTIVE DURING A SHORTED CYLINDER.

(C) BUFFERING SECONDARY AVAILABLE

THE SECONDARY AVAILABLE SIGNAL GENERATED ON THE TRIGGER PRIMARY BD (SEE TRIGGER PRIMARY BD) IS ROUTED THROUGH THE MISCELLANEOUS FUNCTION BD FOR BUFFERING AND LIMITING BEFORE BEING OUTPUTTED TO THE MUX A/D BD (SEE SECTION 5 MUX A/D).

(D) LIMITING PRIMARY AVAILABLE

AS WITH SECONDARY AVAILABLE, PRIMARY AVAILABLE IS ROUTED THROUGH THE MISCELLANEOUS FUNCTION BD FOR LIMITING BEFORE BEING OUTPUTTED TO THE MUX A/D BD (SEE SECTION 5 MUX A/D).

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(E) PRODUCING VAC ANALOG

VAC ANALOG IS PRODUCED USING A VACUUM TRANSDUCER WHICH IS CONNECTED TO THE ENGINE BY MEANS OF A RUBBER TUBE THAT PASSES ALONG THE BOOM (NOTE:THIS TUBE IS MADE OF A CONDUCTIVE RUBBER AND SHOULD NOT BE ALLOWED TO COME INTO CONTACT WITH ELECTRICAL CIRCUITS.)

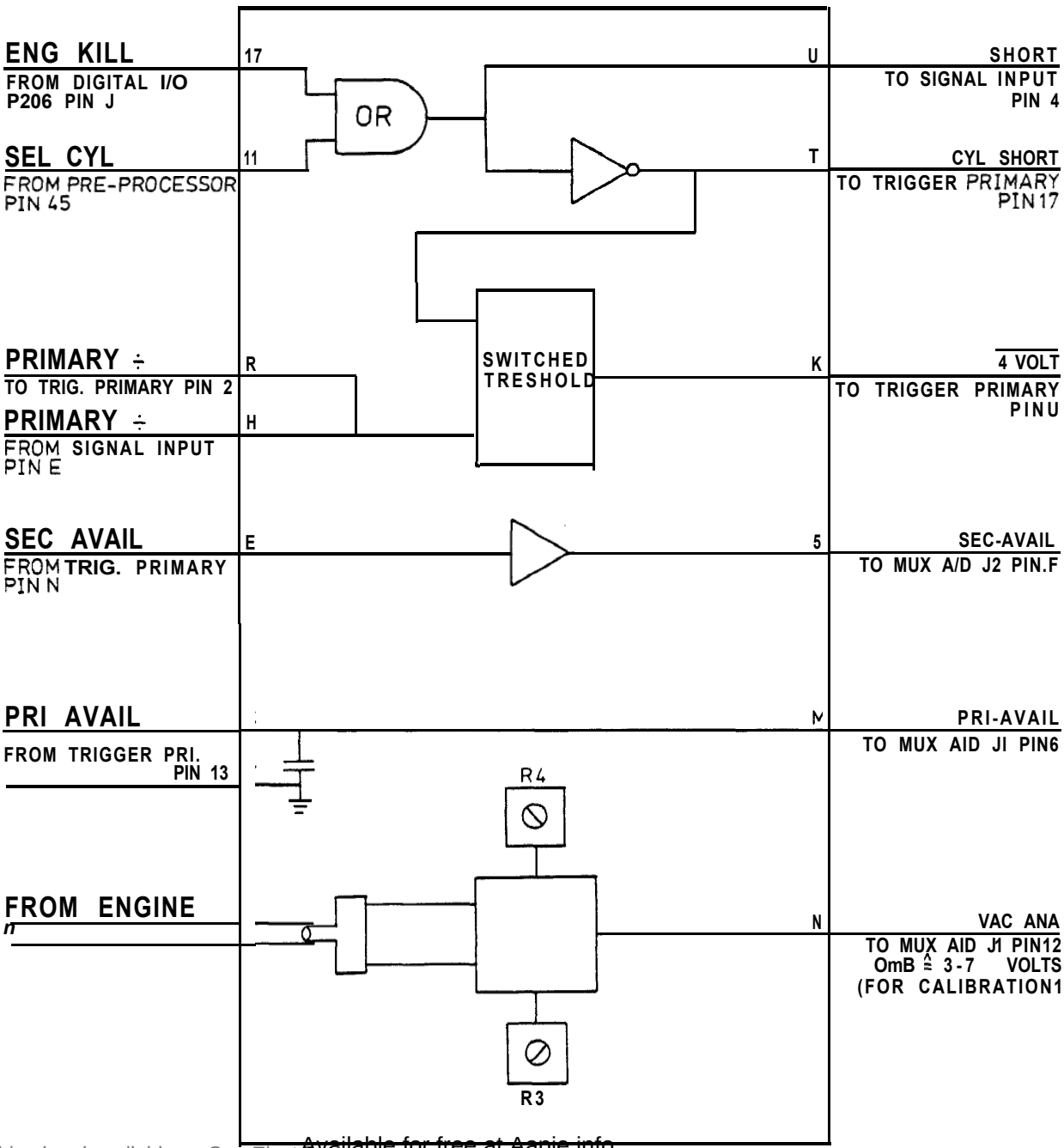
THE OUTPUT OF THE TRANSDUCER IS AMPLIFIED AND OUTPUTTED TO THE MUX A/D FOR DISPLAY BY THE COMPUTER.

THE GAIN AND ZERO FOR THE VACUUM CIRCUIT ARE POSITIONED ON THE MISCELLANEOUS FUNCTION BD. AS WITH ALL SIGNALS TO THE MUX A/D THIS SIGNAL IS LIMITED.

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MISCELLANEOUS FUNCTION BD.

BLOCK DIAGRAM



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WAVEFORMS

NOTE: THE FOLLOWING WAVEFORMS ARE PRODUCED BY THE TESTER WHEN IT IS CONNECTED TO AN IS100A. THE SETTINGS OF THE IS100A AND THE TESTER MUST BE AS FOLLOWS:

IS100A

CONNECT-	PRIMARY KL1
	PRIMARY KL15
	SECONDARY PATTERN
	RED TRIGGER
	ENGINE GROUND
	BATT+

SETTINGS	CYLINDERS	4
	RPM	1000
	ALT/VOLT/OHMS	+12V
	POWER	ON
	IGNITION	ON
	ALL ELSE	OFF

MCS-2000

ALLOW SELF CALIBRATION

GO TO WORKSHOP TEST: SET NO.CYL TO 4

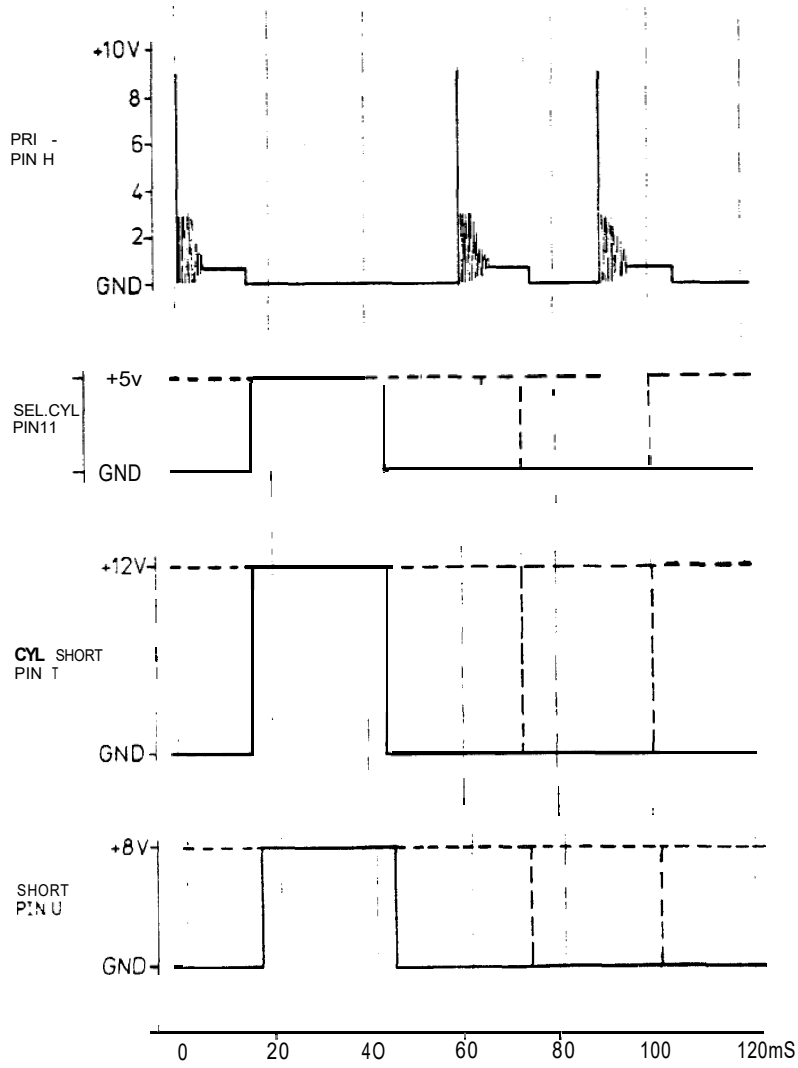
GO TO TEST 8 CYLINDER COMPARISON

NOTE: PRESS * TO INITIATE CYL SHORTING

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MISCELLANEOUS FUNCTION BD.

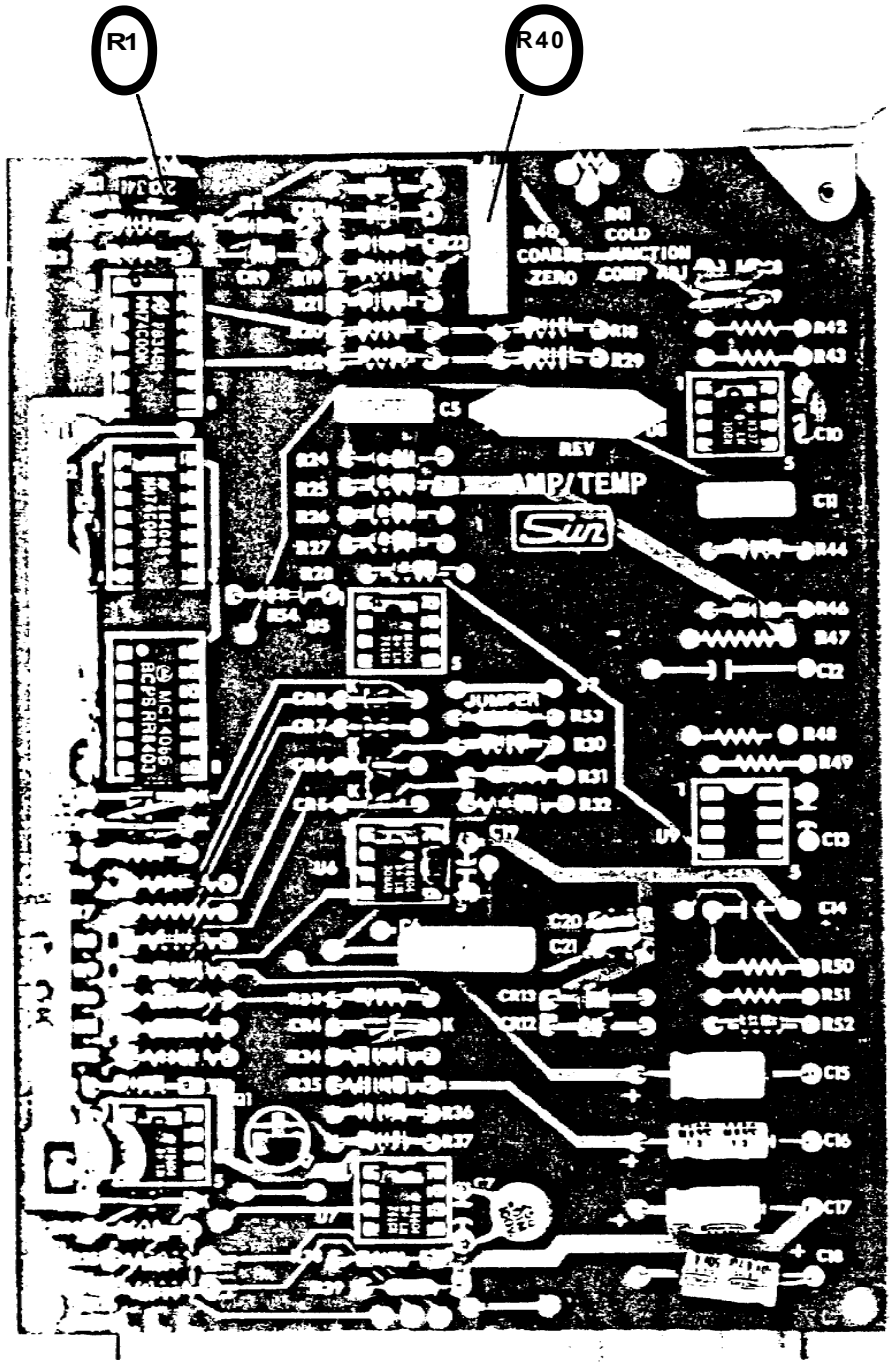
WAVEFORMS



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3.4.8

AMP/TEMP (SLOT 6)



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G. AMP/TEMP B D (SLOT 6)

STARTING/CHARGING AMPS ARE MEASURED BY CLAMPING THE AMP PROBE AROUND THE BATTERY CABLE WITH THE ARROW ON THE PROBE POINTING TOWARDS THE (-) BATTERY TERMINAL. CURRENT SUPPLIED BY THE BATTERY WILL BE READ AS (-) WHILE CHARGING CURRENT INTO THE BATTERY WILL READ AS (+).

THE AMP PROBE CONTAINS A "HALL CHIP" WHICH PRODUCES A VOLTAGE THAT IS PROPORTIONAL TO THE MAGNETIC FLUX SURROUNDING IT. AS THE FLUX INCREASES DUE TO INCREASED CURRENT FLOW THE VOLTAGE PRODUCED BY THE HALL CHIP ALSO INCREASES.

FOR PROPER OPERATION, THE HALL CHIP REQUIRES A CONSTANT CURRENT SOURCE FOR BIAS. THIS IS PROVIDED BY THE AMP CIRCUIT BOARD, VIA ANALOG BACKPLANE AND BOOM CONNECTORS. THE AMOUNT OF CURRENT SUPPLIED IS DETERMINED BY TWO CONTROLS. THE FIRST IS THE PROBE CAL CONTROL ON THE PROBE ITSELF. THIS IS ADJUSTED (CURRENT BIAS) USING AN SRT-28 (REFER TO THE VAT-40) SERVICE MANUAL).
THE SECOND IS THE ZERO CONTROL R40 ON THE AMP CIRCUIT BOARD (REFER TO CHECKOUT + CALIBRATION PROCEDURE SECTION 1).

THE OUTPUT VOLTAGE OF THE HALL CHIP IS APPLIED TO THE AMP CIRCUIT BOARD VIA THE BOOM AND ANALOG BACKPLANE. ON THE AMP BOARD IT IS AMPLIFIED AND CALIBRATED (GAIN CONTROL R1). THE SIGNAL Is FURTHER AMPLIFIED WITH THE AMOUNT OF AMPLIFICATION DETERMINED BY THE SCALE SELECT LINE WHICH ENTERS THE AMP BOARD ON PINS B AND S.

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WHEN THIS SIGNAL IS TAKEN HIGH BY THE DIGITAL I/O BOARD, THE GAIN IS CUT BY A FACTOR OF 10 WHICH RESULTS IN THE SELECTION OF THE 1000 AMP SCALE. WHEN THE LINE IS TAKEN LOW THE 100 AMP SCALE IS SELECTED.

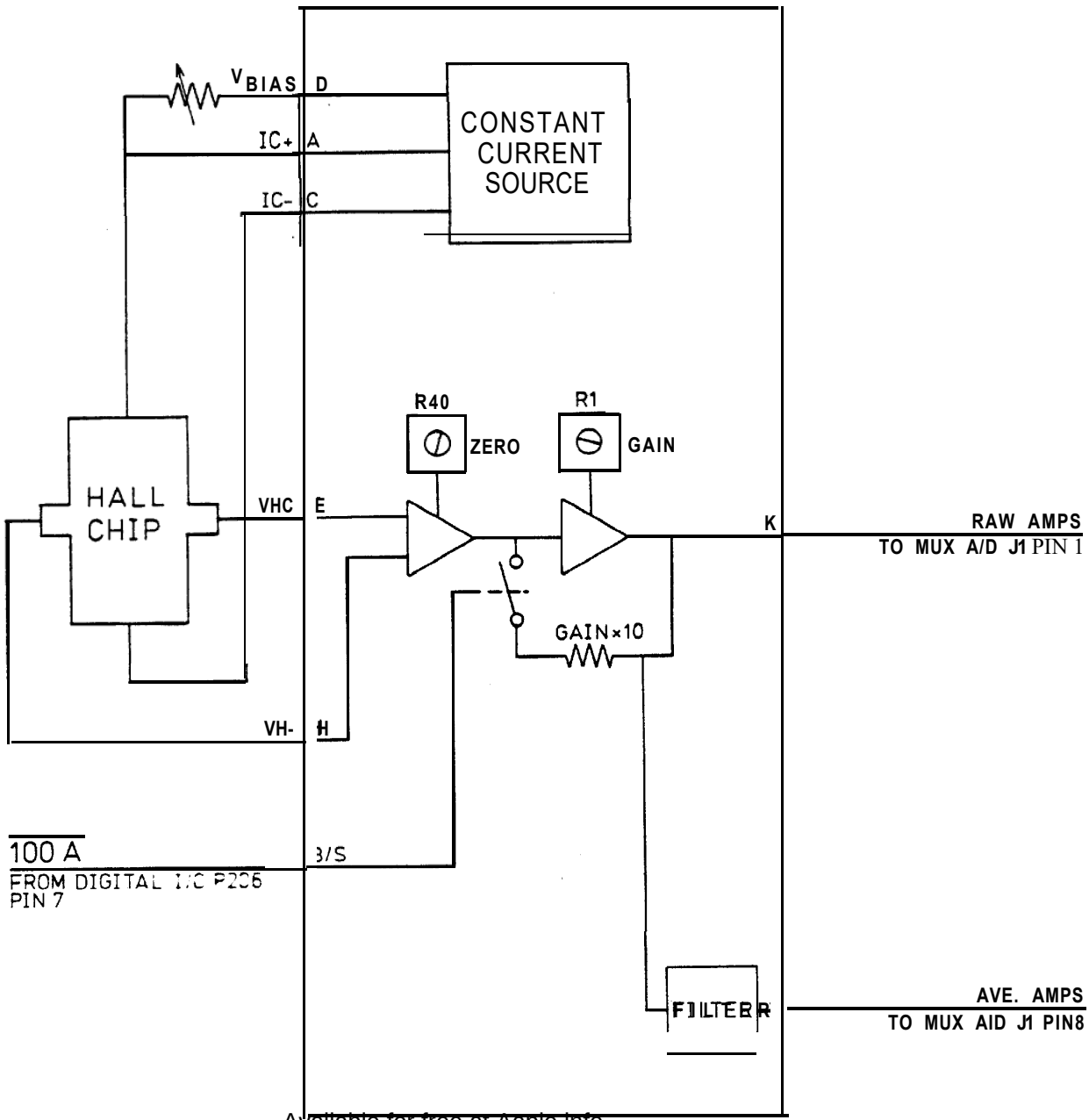
THE RESULTING VOLTAGE, AFTER GAIN SELECTION, IS MADE DIRECTLY AVAILABLE AT PIN K. THIS VOLTAGE QUICKLY RESPONDS TO CHANGES IN CURRENT FLOW. AS SUCH, IT IS USED DURING THE CRANKING TEST TO DETERMINE AMPS PER CYLINDER. THE VOLTAGE AT PIN J IS ALSO PROPORTIONAL TO THE CURRENT. HOWEVER, IT IS FILTERED TO REPRESENT AVERAGE AMPS.

DURING SELF CAL THE CPU MEASURES AND STORES THE "ZERO CURRENT" OFFSET VOLTAGE ON THE 100 AMP SCALE. IT THEN USES THIS ZERO CORRECTION DURING TESTING TO SUBTRACT ZEROING ERRORS OUT OF THE DISPLAYED READINGS. IF DURING SELF TEST THE ZERO IS TOO FAR OUT (±2.0 VOLT) THE MESSAGE "SERVICE REQUIRED" WILL BE DISPLAYED.

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AMP/TEMP BD

BLOCK DIAGRAM



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GENERAL

THE AMP/TEMP BD. WAS MODIFIED TO INCREASE **THE RESOLUTION OF THE AMPS** MEASUREMENTS, AND IMPROVE RAW AMPS READINGS.

METHOD

THE INCREASED RESOLUTION WAS ACHIEVED BY TAKING THE 100/500 AMP LINE AT PIN 8 OF THE AMP/TEMP BD. PERMANENTLY LOW. THIS EFFECTIVELY SETS THE AMP/TEMP BD. TO THE 500 AMP RANGE, INSTEAD OF THE NORMALLY SELECTED 1000 A.

THE RESOLUTION IS THEREFORE INCREASED FROM :

OLD 7 MUX VOLTS/1000AMPS ≙ 7mV/AMP ON THE MUX A/D

TO :

NEW 7 MUX, VOLTS/500 AMPS ≙ 14 mV/AMP ON THE MUX A/D

THE SOFTWARE HAS BEEN CHANGED TO ACCEPT 7 MUX VOLTS AS 500 AMPS.

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IMPORTANT

1. IF AN UNMODIFIED AMP/TEMP BD. IS USED IN COMBINATION WITH THE DISC BASED SOFTWARE THE DISPLAYED AMPS READING WILL BE HALF THE REAL VALUE.
2. IF A MODIFIED BD. IS USED WITH THE OLD SOFTWARE DISPLAYED AMPS READING WILL BE DOUBLE THE REAL VALUE.

THESE BOARDS ARE NOT INTERCHANGEABLE

RAW AMPS

THE ADDITION OF THE 10nF CAPACITOR IN PARALLEL WITH R27 IMPROVES THE PEAK AMP RESPONSE FOR THE RAW AMPS MEASUREMENTS.

CALIBRATION

THE CALIBRATION PROCEDURE OF THE MODIFIED BOARD REMAINS THE SAME AS DETAILED IN THE SUN 2014 SERVICE REPAIR MANUAL SECTION 1 PAGE 17, HOWEVER ALL MUX VOLTAGES MENTIONED SHOULD BE DOUBLED.

CONNECTIONS **CHECK**

DUE TO THE MODIFICATION TO THE AMP/TEMP BD. THE 100 AMP RANGE IS NO LONGER USED DURING THE CONNECTIONS CHECK.

THE CRITERIA FOR CONNECTION REMAINS ± 1 AMP. AS THIS IS NOW CARRIED OUT IN THE 500 AMP RANGE IT CORRESPONDS TO A CONNECTION VOLTAGE OF ± 14 mV AT P903 PIN 8 OF THE MUX A/D, AS OPPOSED TO THE OLD CONNECTION VOLTAGE OF +/- 70 mV

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AUTO ZERO

DURING THE TESTERS SELF CALIBRATION PROCEDURE THE CPU TAKES NEW ZERO'S FOR AMPS. THE FOLLOWING CONDITIONS HAVE TO BE MET OR THE TESTER WILL DISPLAY THE TESTER "SERVICE REQUIRED" FOR "AMPS" MESSAGE.

AVE. AMPS	= +/- 2V ON 100 AMP RANGE = +/- 28.5A = +/- 2V ON 500 AMP RANGE = +/- 144.5A
RAW AMPS	= +/- 2V ON 500 AMP RANGE = +/- 144.5A

ANY VALUES WITHIN THESE LIMITS WILL BE AUTO-ZEROED.

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SECTION 4

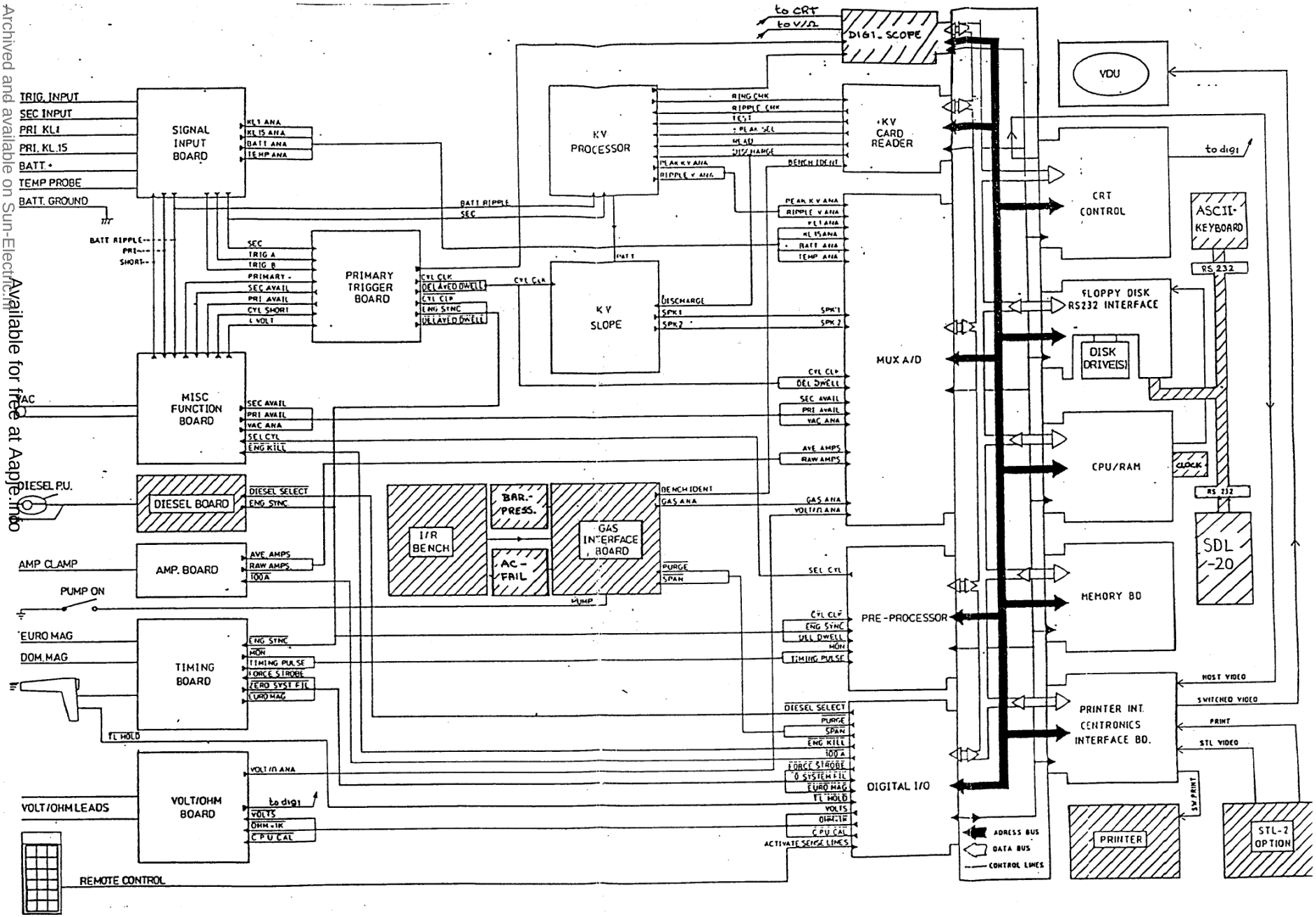
SCHEMATICS

4.1 BLOCK DIAGRAM

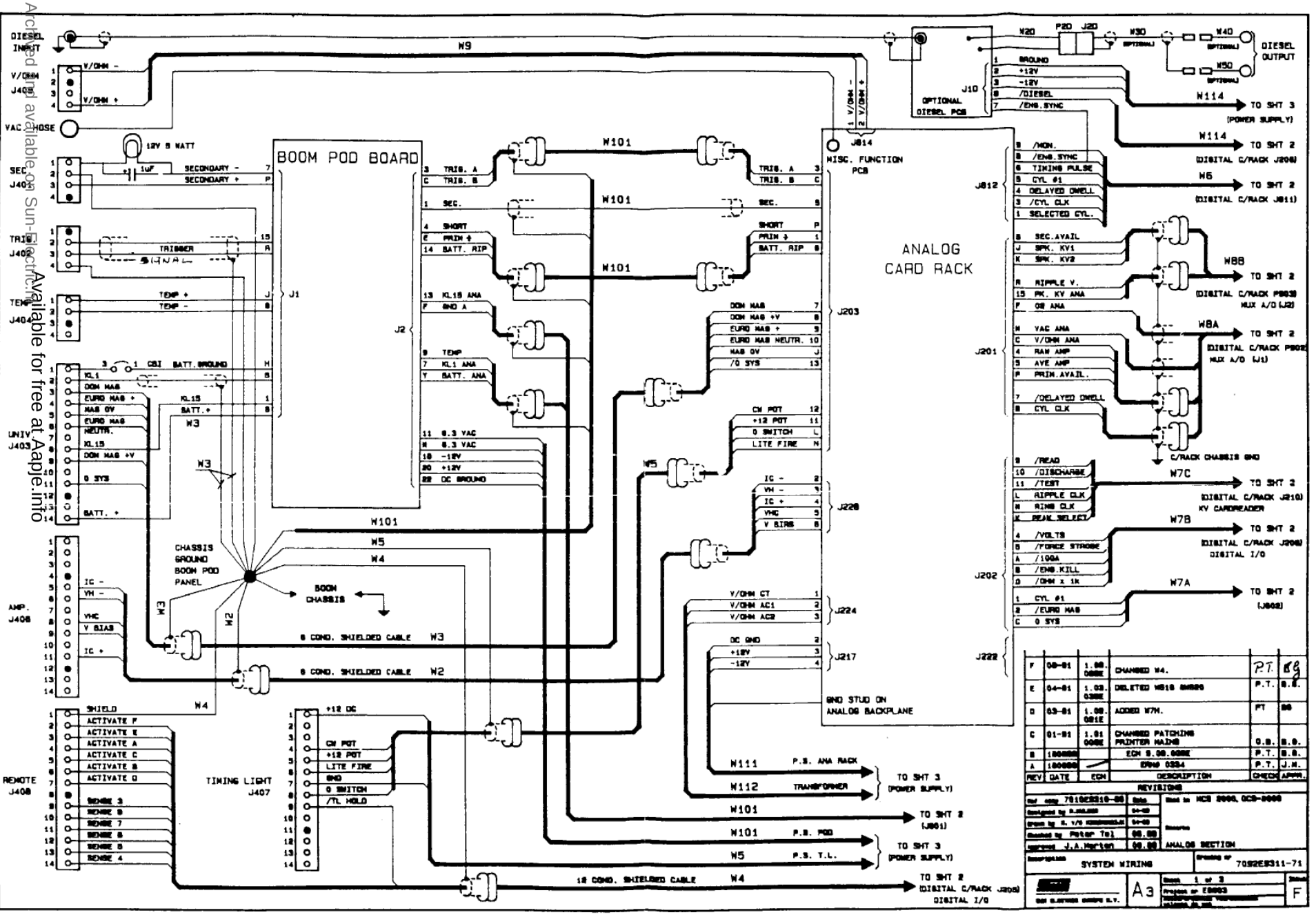
4.2 SYSTEM WIRING

4.3 SCHEMATICS SUB-ASSY'S

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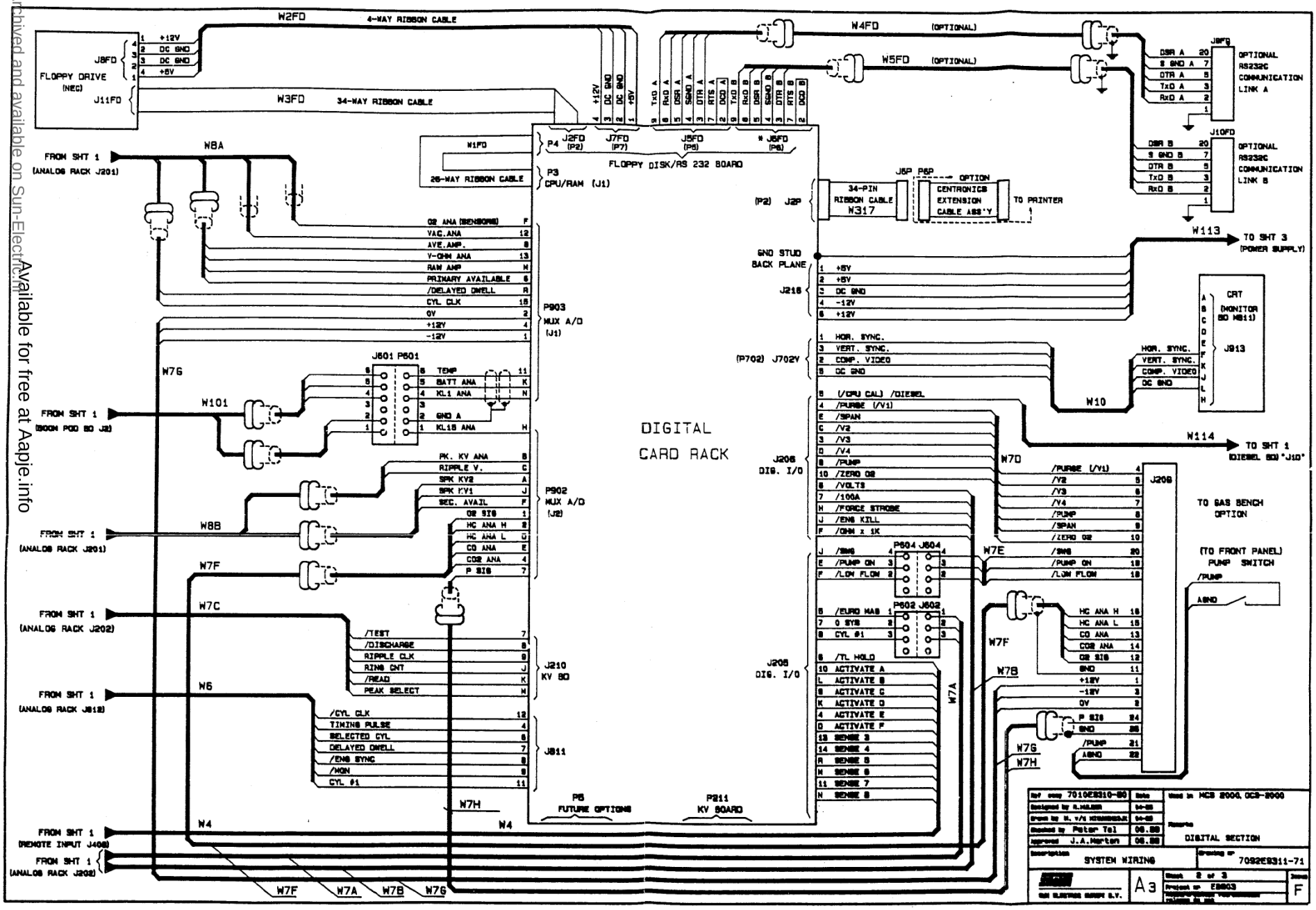
SUN- MCS-2000 BLOCK DIAGRAM. 4.1



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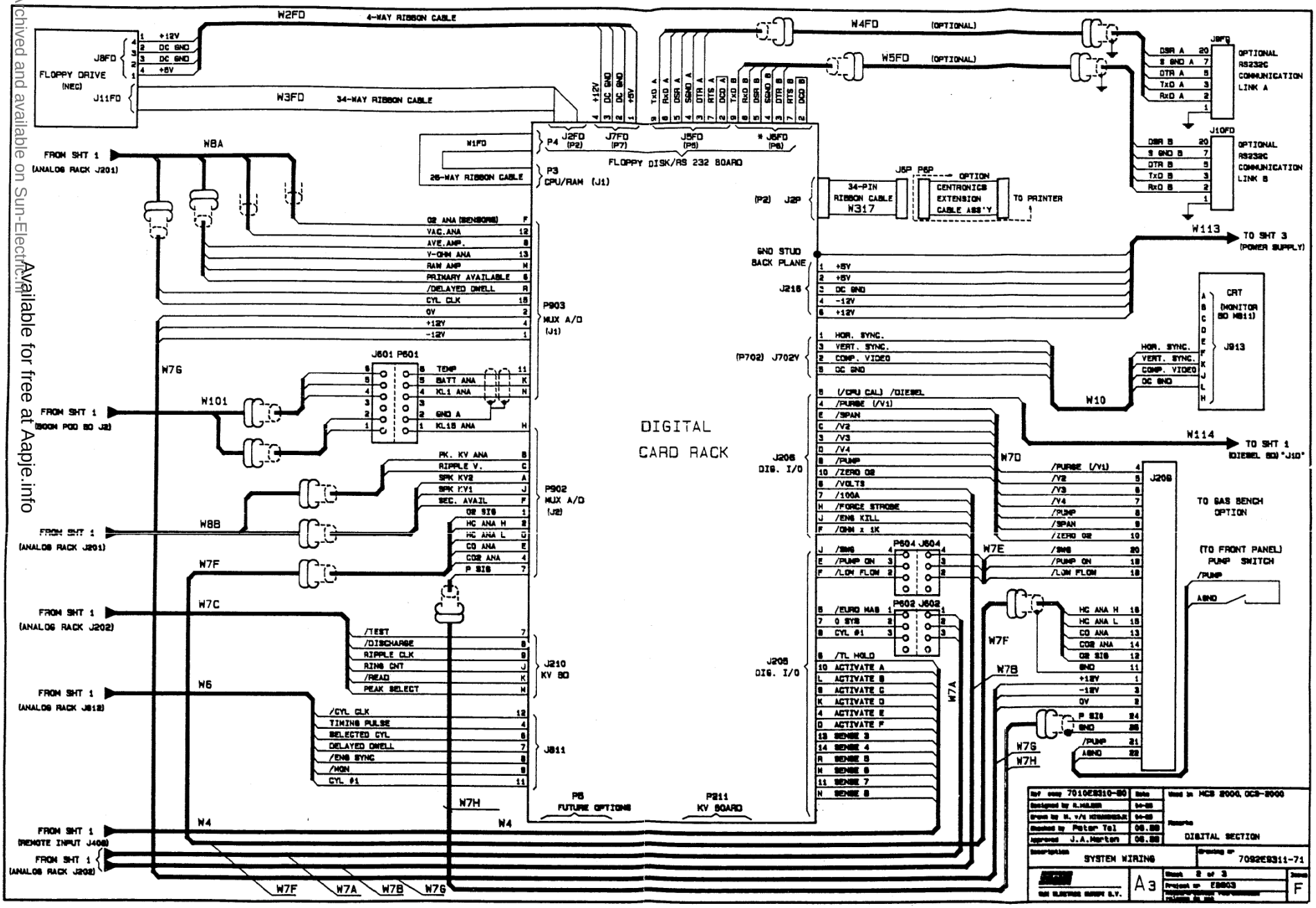


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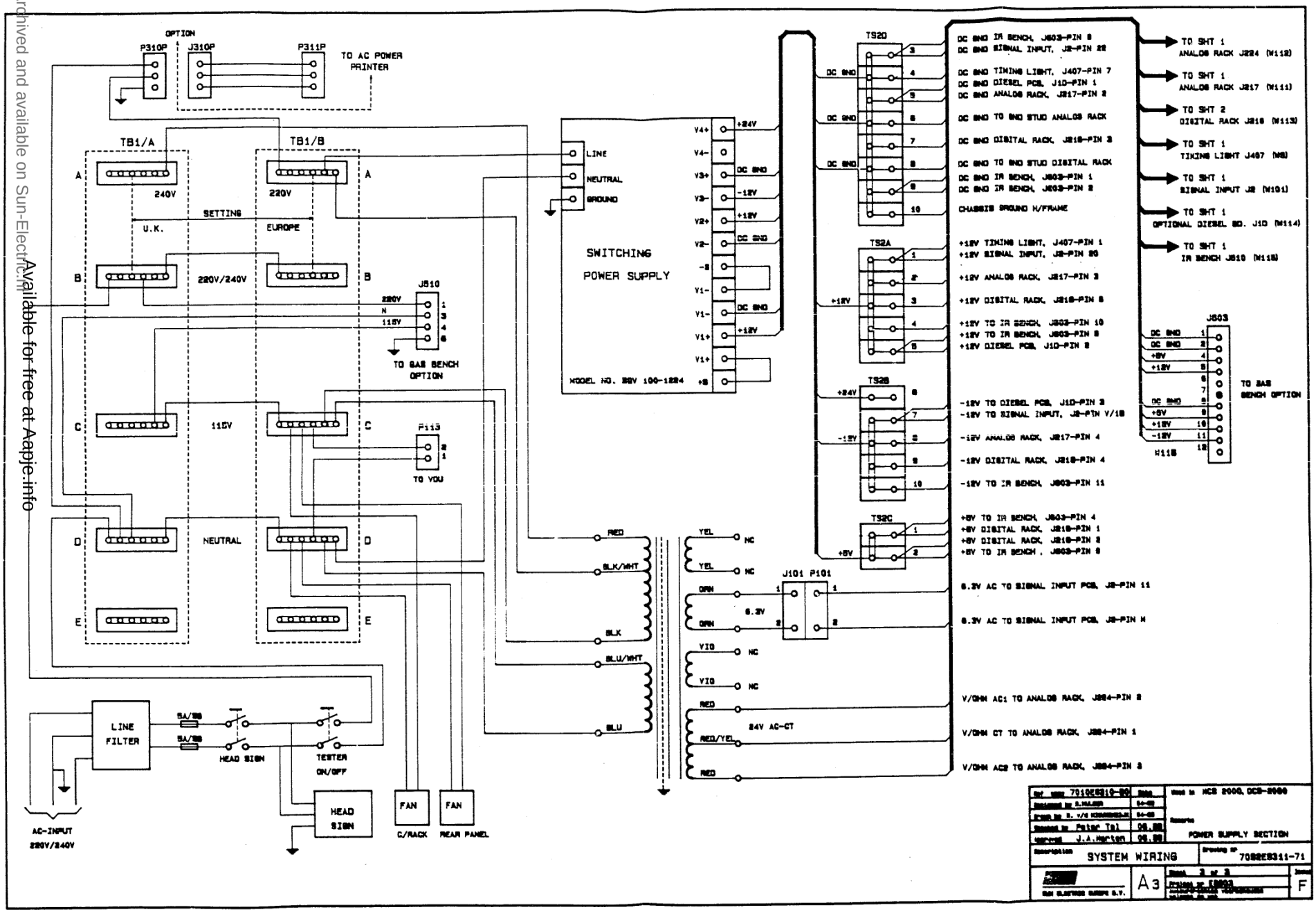


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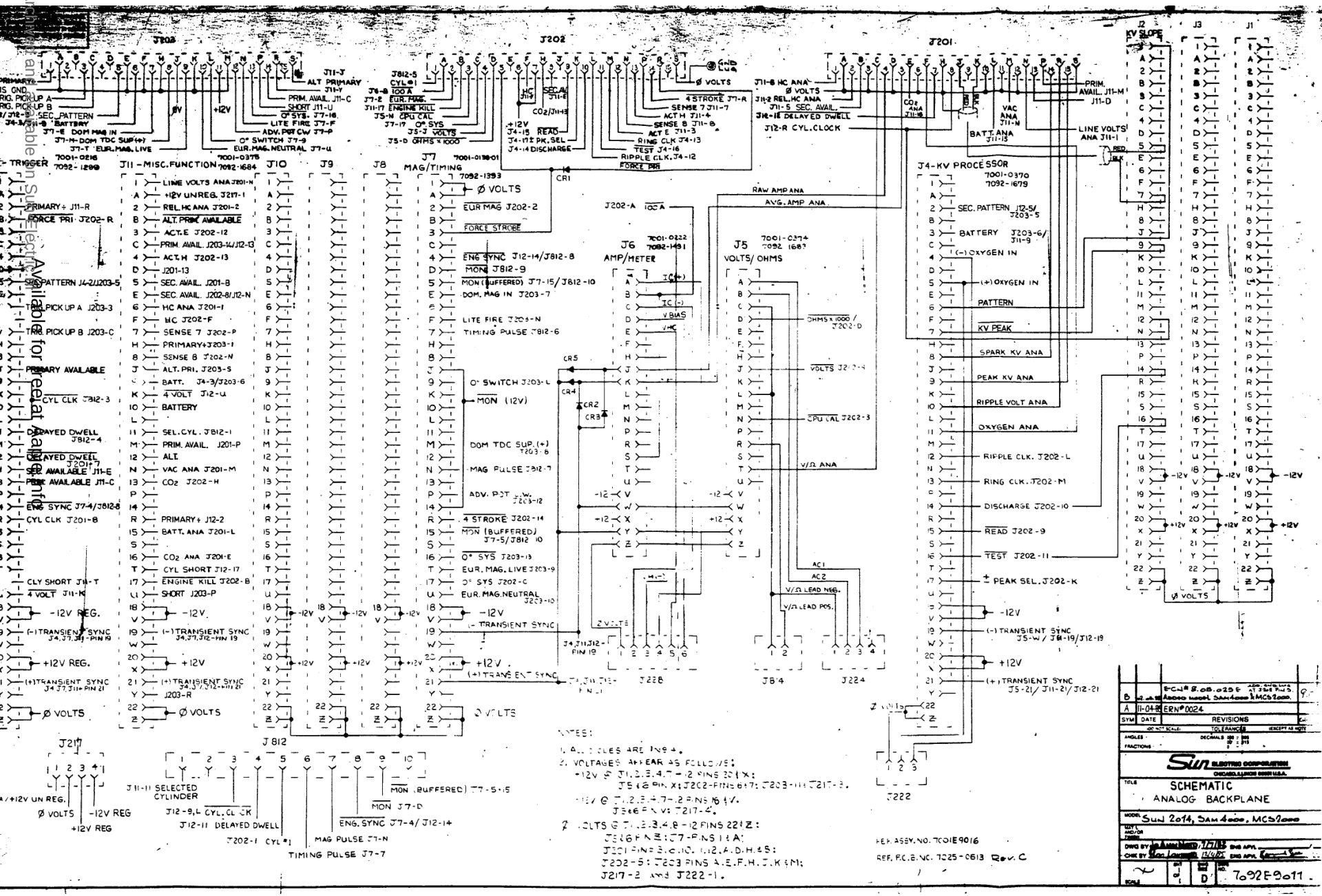
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SUB-ASSY'S FOR MCS-2000SL

ASSY NAME:	*ASSY:*	*SCHEMATIC:*
ANALOG BACKPLANE	7001E9016	7092E9011
KV-SLOPE	7001E9020	7092E9015
KV/O2-PROCESSOR	7001E9310-44	7092E9013
VOLT/OHM	7001E9044	7092E9023
AMP	7001E9310-12	7092E9310-22
TIMING	7001E9045	7092E9024
MISC. FUNCTION	7001E9017	7092E9012
TRIGGER PRIMARY	7001E9019	7092E9014
DIGITAL BACKPLANE	7001E9008	7092E9002
DIGITAL I/O	7001E9010	7092E9004
KV CARD READER	7001E9011	7092E9005
MUX A/D (OLD)	7001E9012	7092E9006
MUX A/D (NEW)	7001E9313-27	7092E9313-27
RAM (MEMORY)	7001E9311-48	7092E9311-51
ECPU68K	7001E9311-44	7092E9311-47
CENTRONICS INTERFACE	700139311-19	7092E9311-18
FLOPPY/RS232 INTERFACE	7001E9310-05	7092E9310-11
ECRT	7001E9311-59	7092E9311-65
PRE-PROCESSOR	7001E9009	7092E9003
REMOTE CONTROL	7009E9316-54	7010E9310-83
POWER SUPPLY SSI/l00W	7009E9310-32	7092E9025
TIMING LIGHT	7001E9311-60	7092E9017
SIGNAL INPUT	7001E9005	7092E9016
KME MONITOR	7009E9313-10	
KME DEFLECTION (OLD)	-------	---
TETRACO POWER/DEFLECTION	20012A	---
KME DEFLECTION (NEW)	7001E9312-61	7092E9312-61
KME LINEAR REGULATOR	7001E9311-50	7092E9311-58
TETRACO POWER/DEFLECTION	7001E9312-16	7092E9312-16
TETRACO CRT BOARD	700139312-17	7092E9312-17
TETRACO VDU HARNESS W10	7076E9321-35	
TETRACO TUBE 20 INCH SPEC	7096E4057-64	
TETRACO YOKE 20 INCH SPEC	7009E9317-02	
TETRACO MONITOR SPEC	7096E4056-99	

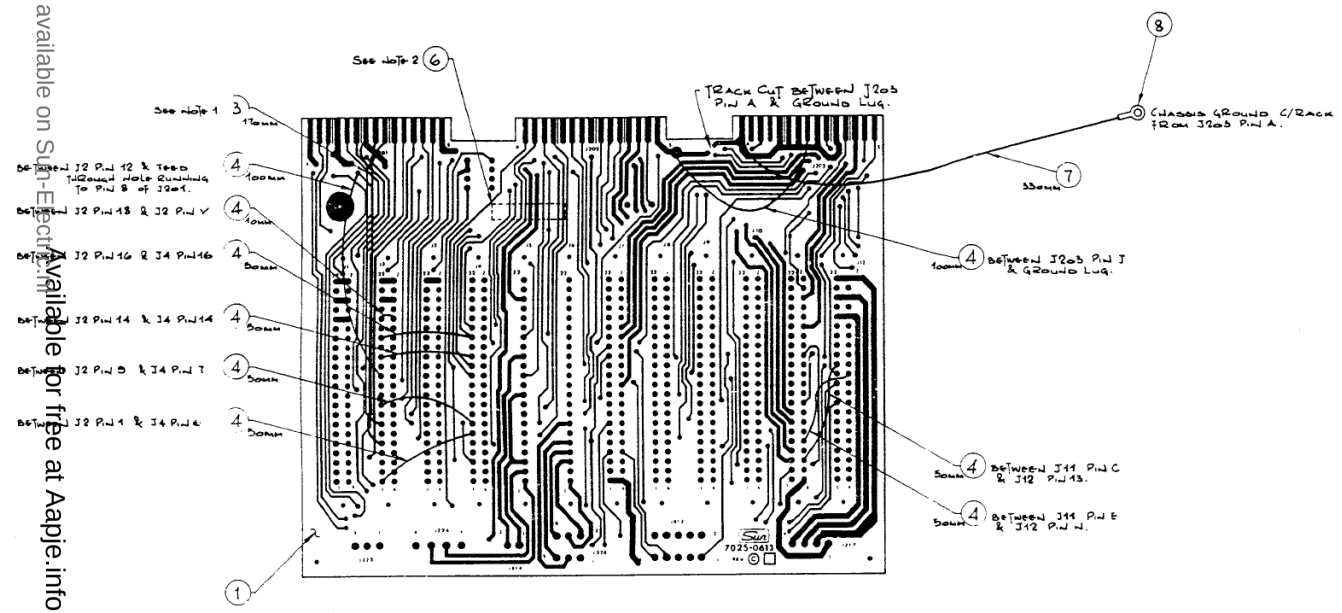
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J703
J702
J701
J2 KV SLOPE
J3
J1
J11 - MISC. FUNCTION
J10
J9
J8
J7 MAG/TIMING
J6 AMP/METER
J5 VOLTS/OHMS
J4 - KV PROCESSOR
J812
J217
J222
J228
J224
J224
TRIGGER
PRIMARY+ J11-R
FORCE PRI J202-R
SEC. PATTERN J4-2/J203-5
TRIG. PICK UP A J203-3
TRIG. PICK UP B J203-C
PRIMARY AVAILABLE
CYL CLK J812-3
DELAYED DWELL J812-4
DELAYED DWELL J201-7
SEC AVAILABLE J11-E
PRIM AVAILABLE J11-C
ENG SYNC J7-4/J812-8
CYL CLK J201-8
CLY SHORT J11-T
4 VOLT J11-K
-12V REG.
(-) TRANSIENT SYNC J4,J7,J11-PIN 19
+12V REG.
(+) TRANSIENT SYNC J4,J7,J11-PIN 21
Ø VOLTS
LINE VOLTS ANA J201-N
+12V UNREG. J217-1
REL HC ANA J201-2
ALT. PRIM AVAILABLE
ACT E J202-12
PRIM. AVAIL. J203-14/J12-13
ACT H J202-13
J201-13
SEC. AVAIL. J201-8
SEC. AVAIL. J202-8/J12-N
HC ANA J201-1
HC J202-F
SENSE 7 J202-P
PRIMARY+ J203-1
SENSE 8 J202-N
ALT. PRI. J203-S
BATT. J4-3/J203-6
4 VOLT J12-U
BATTERY
SEL. CYL. J812-1
PRIM. AVAIL. J201-P
ALT.
VAC ANA J201-M
CO2 J202-H
PRIMARY+ J12-2
BATT. ANA J201-L
CO2 ANA J201-E
CYL SHORT J12-17
ENGINE KILL J202-B
SHORT J203-P
-12V.
(-) TRANSIENT SYNC J4,J7,J12-PIN 19
+12V
(+) TRANSIENT SYNC J4,J7,J12-PIN 21
J203-R
Ø VOLTS
Ø VOLTS
EUR MAG J202-2
FORCE STROBE
ENG SYNC J12-14/J812-8
MON J812-9
MON (BUFFERED) J7-15/J812-10
DOM. MAG IN J203-7
LITE FIRE J203-N
TIMING PULSE J812-6
O° SWITCH J203-L
MON (12V)
DOM TDC SUP. (+) J203-6
MAG PULSE J812-7
ADV. POT J203-12
4 STROKE J202-14
MON (BUFFERED) J7-5/J812-10
O° SYS J203-13
EUR. MAG. LIVE J203-9
O° SYS J202-C
EUR. MAG. NEUTRAL J203-10
-12V
(-) TRANSIENT SYNC
+12V
(+) TRANS ENT SYNC
J4,J11,J12-PIN 21
Ø VOLTS
RAW AMP ANA
AVG. AMP ANA
J202-A 100A
IC (+)
IC (-)
V BIAS
VHC
OHMS X 1000 / J202-D
VOLTS J202-A
CPU CAL J202-3
V/Ω ANA
AC1
AC2
V/Ω LEAD NEG.
V/Ω LEAD POS.
2 VOLTS
Ø VOLTS
7001-0222
7092-1491
7001-0374
7092-1683
7001-0370
7092-1679
SEC. PATTERN J12-5/J203-5
BATTERY J203-6/J11-9
(-) OXYGEN IN
(+) OXYGEN IN
PATTERN
KV PEAK
SPARK KV ANA
PEAK KV ANA
RIPPLE VOLT ANA
OXYGEN ANA
RIPPLE CLK. J202-L
RING CLK. J202-M
DISCHARGE J202-10
READ J202-9
TEST J202-11
± PEAK SEL. J202-K
-12V
(-) TRANSIENT SYNC J5-W / J11-19/J12-19
+12V
(+) TRANSIENT SYNC J5-21/ J11-21/J12-21
Ø VOLTS
J11-J ALT PRIMARY J11-Y
PRIM. AVAIL. J11-C
SHORT J11-U
O° SYS. J7-18
LITE FIRE J7-F
ADV. POT CW J7-P
O° SWITCH J7-9
EUR. MAG. NEUTRAL J7-U
EUR. MAG. LIVE J7-T
7001-0216
7092-1299
7001-0376
7092-1684
J812-5 CYL #1
J7-2 EUR TRIG
J7-17 ENGINE KILL
J5-N CPU CAL
J7-17 O° SYS
J5-J VOLTS
J5-D OHMS X 1000
7001-0138-01
7092-1393
CR1
CR2
CR3
CR4
CR5
HC J11-F
SEC AV J11-E
CO2/J11-S
+12V J4-15 READ
J4-17 PK. SEL
J4-14 DISCHARGE
4 STROKE J7-R
SENSE 7 J7-7
ACT H J11-4
SENSE 8 J11-8
ACT E J11-3
RING CLK J4-13
TEST J4-16
RIPPLE CLK. J4-12
FORCE PRI
Ø VOLTS
J11-8 HC ANA
Ø VOLTS
J11-2 REL HC ANA
J11-5 SEC. AVAIL.
J12-E DELAYED DWELL
J12-R CYL. CLOCK
CO2 ANA J11-19
VAC ANA J11-N
BATT. ANA J11-15
PRIM. AVAIL. J11-M
J11-D
LINE VOLTS ANA J11-1
RED
BLK
-12V
+12V
Ø VOLTS
J217
Ø VOLTS
-12V REG
+12V REG
+12V UN REG.
J812
J11-11 SELECTED CYLINDER
J12-9, L CYL CL CK
J12-11 DELAYED DWELL
J202-1 CYL #1
TIMING PULSE J7-7
MAG PULSE J7-N
ENG. SYNC J7-4/ J12-14
MON J7-D
MON (BUFFERED) J7-5-15
J222
2 VOLTS
NOTES:
1. ALL DIODES ARE IN914.
2. VOLTAGES APPEAR AS FOLLOWS:
+12V @ J1,2,3,4,7-12 PINS 20 & X:
J5 & PIN X; J202-PINS 6 & 7; J203-11 & J217-3.
-12V @ J1,2,3,4,7-12 PINS N & V:
J5 & PIN V; J217-4.
2 VOLTS @ J1,2,3,4,8-12 PINS 22 & Z:
J5 & PIN B; J7-PINS 11 & A;
J201-PINS B, C, N, 12, A, D, H & S;
J202-5; J203 PINS A, E, F, H, J, K & M;
J217-2 AND J222-1.
REF. ASSY. NO. 7001E9016
REF. P.C.B. NO. 7025-0613 Rev. C
ECN# 8.05.025E
A 11-04-85 ERN# 0024
REVISIONS
SCHEMATIC
ANALOG BACKPLANE
SUN 2014, SAM 4000, MCS2000
DWG BY
CHK BY
7092E9011
D

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A	16-11-87	—	ERN#0103	P.T.

SOLDER-SIDE



NOTES:

1. CONNECT 2-CORE SCREENED CABLE (ITEM 3) AS PER WIRE TABLE:

COLOUR	FROM	TO
RED	J2-5	J201-J
BLACK	J2-7	J201-K
SCREEN	CUT BACK	J201-H

2. ADD LABEL IDENT (ITEM 6) ON COMPONENT SIDE OVER OLD ASS'Y NO. AS SHOWN.

8	1	000 3931-824	RING TERMINAL M5	
7	330mm	000 3.0687.626	WIRE 0.75 mm² GRN/YELL.	
6	1	000 3.0675-563	LABEL IDENT (7001-5016 REV A)	
5				
4	46 mm	000 3.0687.655	WIRE LINK BLACK 22 AWG	
3	170mm	662.0170.000	CABLE SCREENED, 2-CORE	
2				
1	1	7001-0577	PCB ASS'Y ANALOG BACKPLANE	REV. E

N.T.S. SUN 2/14, SAM 4/000, MC6 9/000

P. Tel		
Tim A Scott M.	16.11.87	
Peter Tel	11.05.88	
Norman Gee	17.5.88	

REF D/M# 0607C/34
REF MOD. INSTR # 06025-3305-73
REF PCB# 7025-0613 REV. C
REF SCHEM # 70025-5011

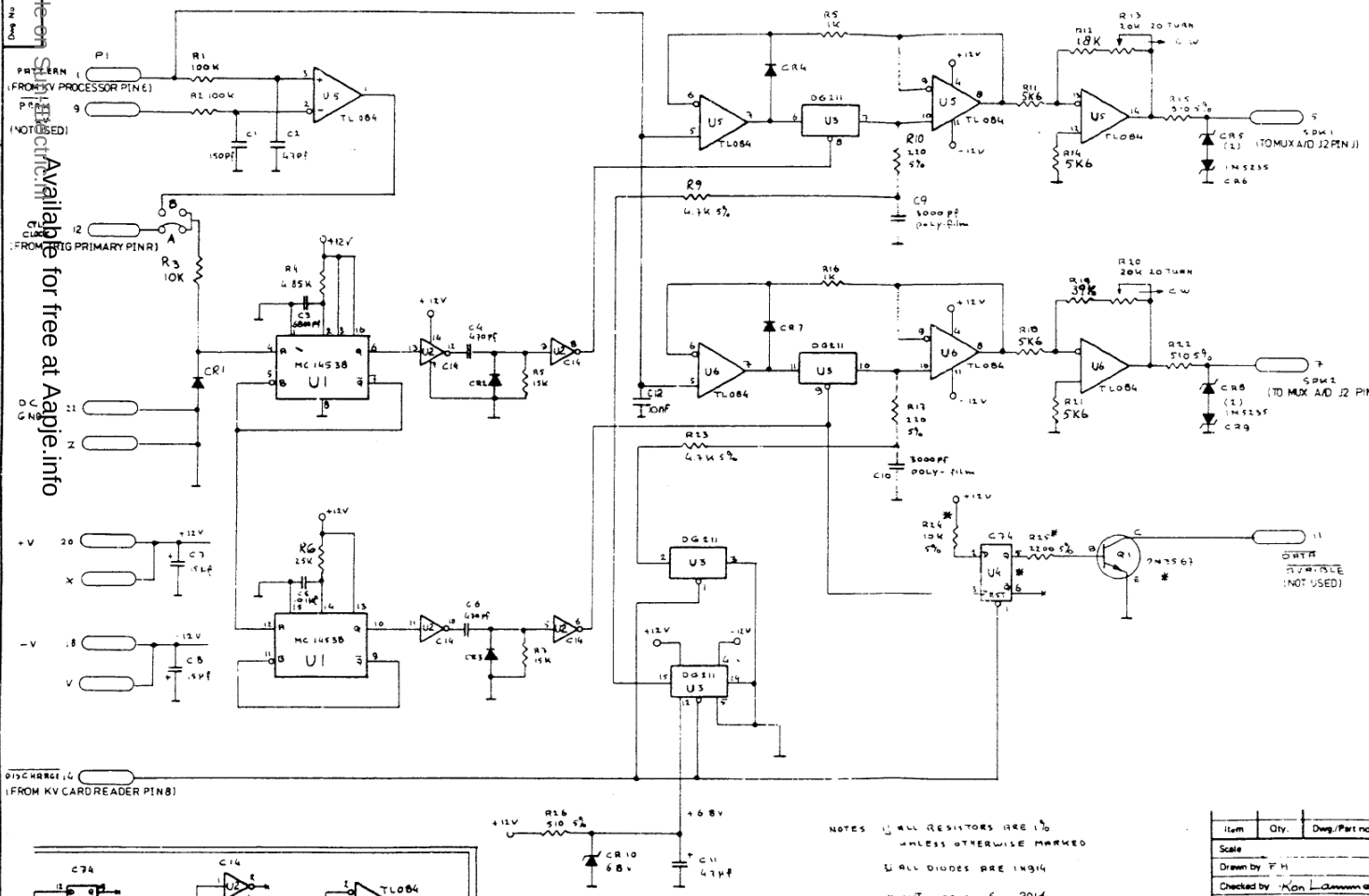
PRINTED CIRCUIT BOARD ASS'Y/ANALOG BACKPLANE 7001-5016

Sun A1 1 1 A

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Available for free at Aapje.info

Hole Schedule		
Code	Qty.	Dia.

Revisions					
Sym.	Date	ECN	Description	Check	Appr.
A	11.04.85		ERN # 0024		



NOTES 1) ALL RESISTORS ARE 1% UNLESS OTHERWISE MARKED

2) ALL DIODES ARE IN914

* NOT USED ON SUN 2014

LAST USED NO. R26, C12, Q1, U6, CR10

REF. ASSY NO. 7001E9020
PCB NO. 7025E9003

Item	Qty.	Dwg./Part no.	Description	Mat'l Spec.	Remarks
Scale		Date	Remarks: USED ON SUN 2014		
Drawn by F.H.		21-02-84			
Checked by Ron Lammers		12-04-85			
Approved Bernard Gar		15-04-85	Finish		

Unless otherwise specified: Dimensions are in mm., Tolerances on: Angles ± 0.5° Holes ± 0.1 Rest ± 0.5

Description: KV SLOPE

Dwg. no: 7092E9015

Sun Electric Europe Amsterdam

Auteursrecht voorbehouden volgens de wet

A2

Sheet of

Code

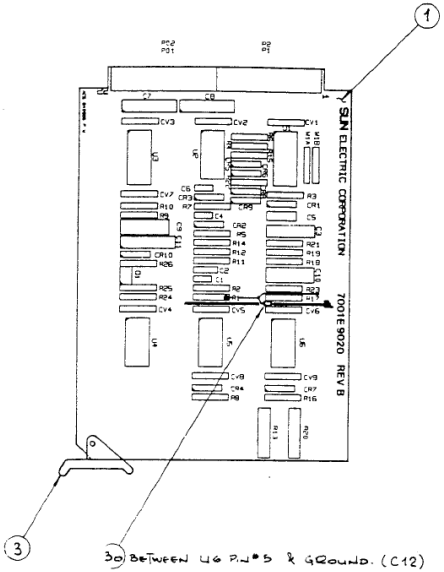
Project no

Issue: A

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Rev	Date	E.C.N.		
B	27.10.87	—	ERN° 0109	P.T. 89



30 BETWEEN U6 PIN°5 & GROUND. (C12)

50				
49				
48	1	0668.0301.000	JUMPER WIRE LINK INSULATED	W1A
47				
46	2	3.0776.617	I.C., TL 084	U5, U6
45	1	3.0776.657	I.C., DG 211 CJ	U3
44	1	3.0776.660	I.C., 74C14 N	U2
43	1	3.0776.650	I.C., MC14538 B	U1
42				
41				
40	5	0803.9235.000	DIODE, ZENER, 1N5235B, 6V8, ½W	CR5, CR6, CR28-CR31
39				
38	5	0771.0272.000	DIODE, 1N914B	CR1-4, CR7
37				
36				
35	2	0679.0414.000	CAPACITOR, 15µ, TANT, 20V	C7, C8
34	1	0679.0513.000	CAPACITOR, 4µ7, ELEC., 16V	C11
33				
32				
31	9	0860.0112.000	CAPACITOR, 0.1µ, 50V, -20+80%	CV1-CV9
30	1	0860.0097.000	CAPACITOR, 10n, C6R, 100V	C12
29	1	0679.1313.000	CAPACITOR, 10n, NUG, 100V	C5
28	1	3.0679.733	CAPACITOR, 6n8, MICA, 100V	C3
27	2	3.0679.726	CAPACITOR, 3n, FILM/MICA, 400V	C9, C10
26	2	3.0679.729	CAPACITOR, 470p, MICA, 400V	C4, C6
25	1	3.0679.730	CAPACITOR, 150p, MICA, 400V	C1
24	1	3.0679.728	CAPACITOR, 47p, MICA, 500V	C2
23				
22	2	0680.1111.000	RESISTOR, VARIABLE, 20K, MULTI-TURN	R13, R20
21				
20	2	3.0670.581	RESISTOR, 100K, ¼W, 1%	R1, R2
19	1	1670.2494.000	RESISTOR, 24K9, ¼W, 1%	R6
18	2	3.0670.577	RESISTOR, 15K, ¼W, 1%	R5, R7
17	1	1670.4873.000	RESISTOR, 4K87, ¼W, 1%	R4
16	2	3.0670.564	RESISTOR, 1K, ¼W, 1%	R8, R16
15				
14				
13	1	3.0680.651	RESISTOR, 33K, ¼W, 5%	R19
12	1	3.0680.599	RESISTOR, 18K, ¼W, 5%	R12
11	1	3.0680.603	RESISTOR, 10K, ¼W, 5%	R3
10	4	3.0680.647	RESISTOR, 5K6, ¼W, 5%	R11, R14, R18, R21
9				
8	2	3.0680.600	RESISTOR, 4K7, ¼W, 5%	R9, R17
7	3	3.0680.747	RESISTOR, 510Ω, ¼W, 5%	R15, R22, R23
6	2	3.0680.606	RESISTOR, 22Ω, ¼W, 5%	R10, R17
5				
4				
3	1	0681.0802.006	CARD EXTRACTOR	
2				
1	1	7a7256 3003.000	PRINTED CIRCUIT BOARD	
Item	Qty.	Dwg. Part No.	Description	

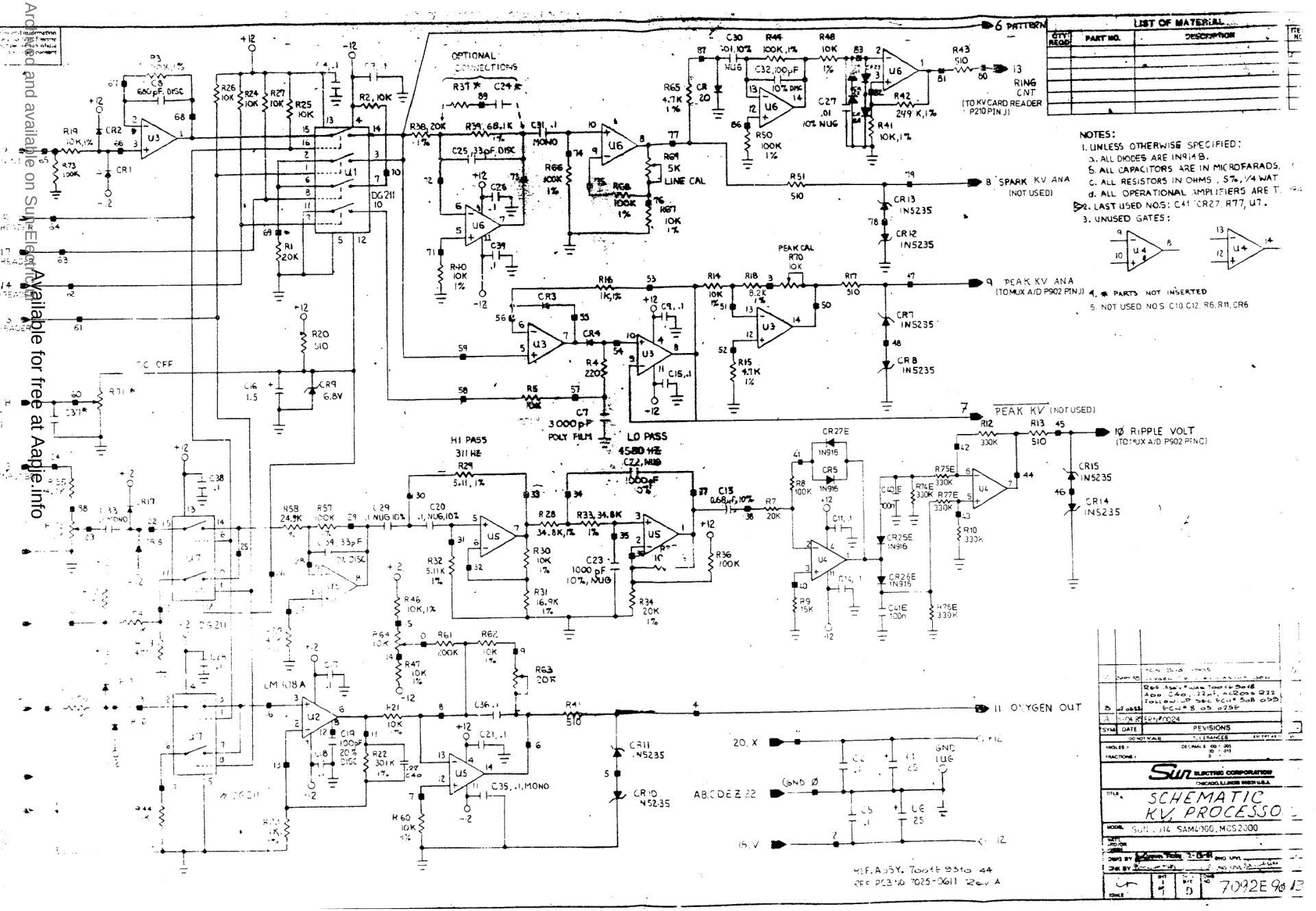
Scale: N.T.S.	Date:	Used on: SUN2014, SUN4000, MCA2000	
Designed by: ACS B.V.	27.05.84		
Drawn by: J.W.A. Smit M.	6.11.87		
Traced by: Peter Tol	11.05.88		
Approved: Bernard Ga.	17.5.88		

Ref B/M° 0610C/86

Ref Schem° 7a928 3015-000

Description: PRINTED CIRCUIT BOARD ASS'Y KV SLOPE			7001E 9020
Sun	A1	Scale: 1:1	B

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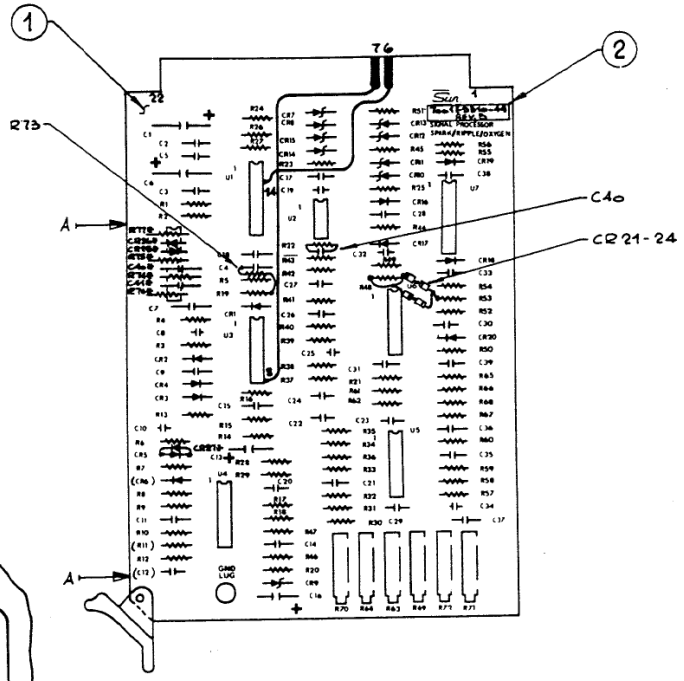


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Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr
A	07.1087		PRELIMINARY		
B	07.1087	—	ERN# 0109 ADD. QTY. ITEM 4, 450mm TO CORRECT DWG. ONLY QTY ITEM 3 WAS 4.	P.T.	BJ

LEGEND



DETAIL A-A

NOTES:
1. REMOVE & DISCARD R6, R8-R12, R18, R70, C10, C12 & CR6.
2. ADD JUMPER WIRES AS SHOWN ON LEGEND & IN DETAIL A-A.
3. REF. DESIGNATIONS BETWEEN ( ) ARE NOT INSERTED.

Item	Qty	Dwg Part no	Description	Remarks
10	1	3.0685.554	RESISTOR, VARIABLE, 10K, 15 TURN	R70
9	450mm	3.0637.655	JUMPER WIRE 22 AWG BLACK	
8	2	3.0679.563	CAPACITOR, 100nF, FILM MMKO	C40E, C41E
7	3	0771-0212	DIODE, 1N914 B	CR25E-CR27E
6	1	1670.8203	RESISTOR, 8K2, ¼W, 1%	R18
5	6	3.0680.659	RESISTOR, 330K, ¼W, 5%	R10, R12, R74E-77E
4	1	1670.1005	RESISTOR, 100K, ¼W, 1%	R8
3	1	1670.1504	RESISTOR, 15K, ¼W, 1%	R9
2	1	3.0657.563	LABEL IDENT (7001E9310-44.)	REV. 'B'
1	1	7001-0370	PCB ASS'Y SAM. PROC. 'REV. D'	

Scale N.T.S.
Drawn by Jim A Soe M. — Date 18.11.87
Checked by Peter Tal — 11.05.88
Approved Bernard Gor — 17.5.88
Remarks: SUN 2014, SAM 4000, MCG 2000.
Finish

Unless otherwise specified: Tolerances: Fractional ± Angular ± Two Place Decimal ± Three Place Decimal ± Material

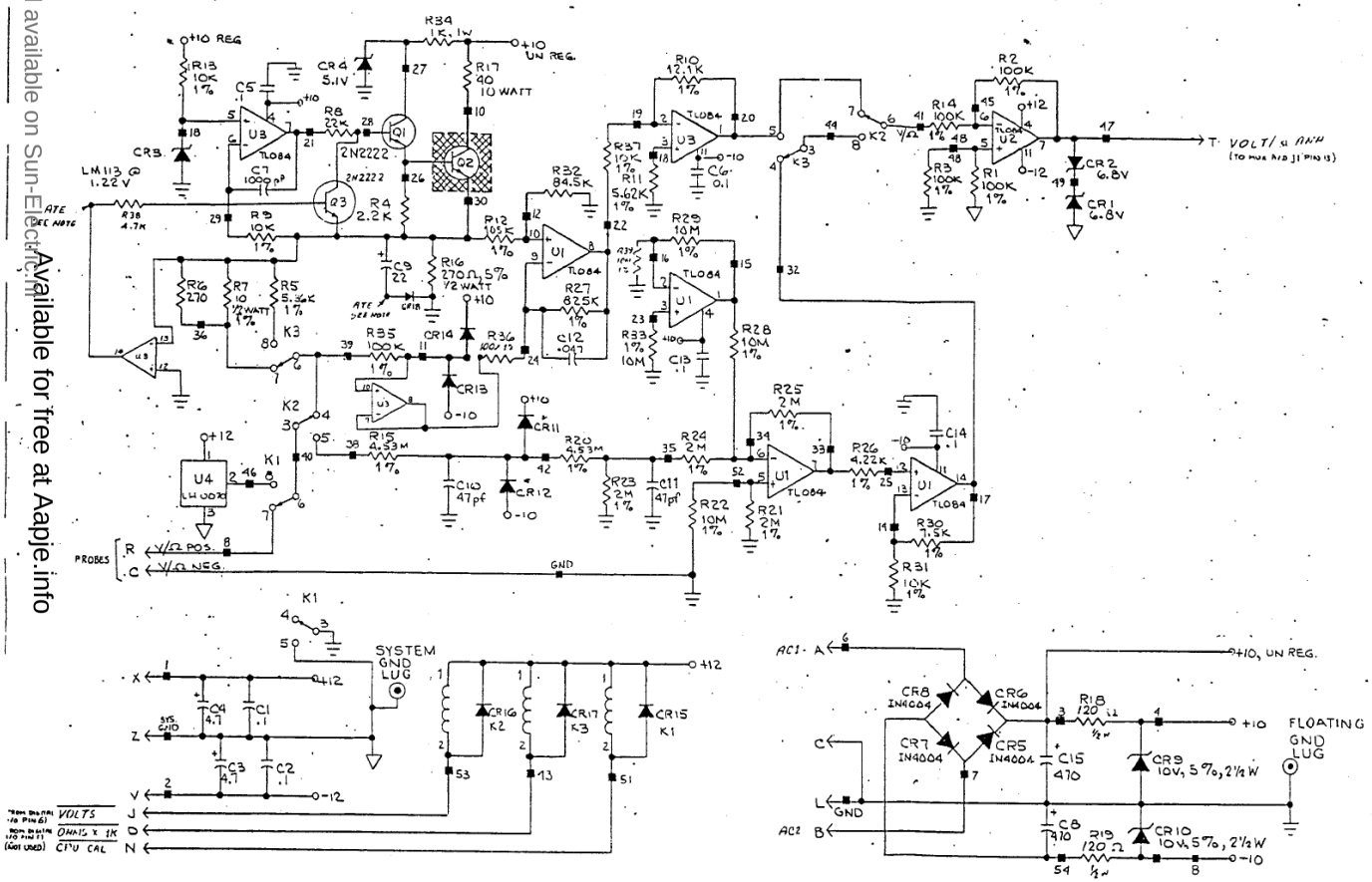
PRINTED CIRCUIT BOARD ASS'Y
KV/02 - SIGNAL PROCESSOR

7001E9310-44

Sun | A2 | Sheet 1 of 1 | Issue B

REF. B/M# 0600C/5a
REF. MOD. INSTR.# 0692E9305-66
REF. PCB# 7025-0611 REV. A
REF. SCHEM# 7092E9013

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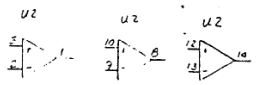


NOTE:

1. UNLESS OTHERWISE SPECIFIED
   - A. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
   - B. ALL CAPACITORS ARE IN MICRO-FARADS
   - C. ALL DIODES ARE IN914
2. LAST USED REF DESIGNATIONS: R39, C15, CR18, U4, Q3, K3
3. UNUSED REF. DESIGNATIONS NONE
4. ALL RELAYS ARE SHOWN IN NORMALLY CLOSED POSITION

* THESE NOT INSERTED

UNUSED GATES



NOTE TO ATE

R38, C39, CR18 AND Q3 ARE ADDED (REWORKED) ON THE COMPONENT SIDE FOR THE REV. 'A' OF 7025-0615. THE NODES INDICATED WILL NOT VISIBLE FOR TESTING.

REVISION RECORD		

REF. ASSEMBLY NO. 7025-0615
PCB NO. 7025-0615

REVISIONS			
B	05-19-87	ECN # 7-10-0616 CR9, CR10 were 1W Zener Diodes	
A	11-04-82	ERN # 0024	

Sun ELECTRIC CORPORATION

SCHEMATIC
VOLT/OHM CIRCUITRY

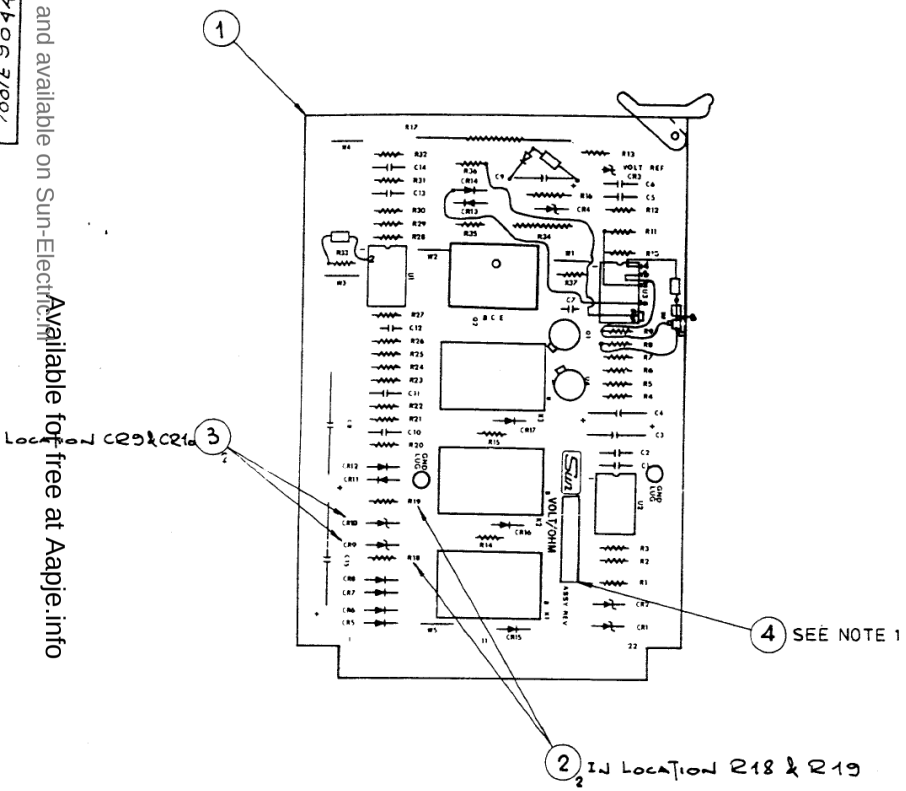
SUN 2014, SUN 4000, MC5 2000

SIZE D — 7025-0615

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Available for free at Aapje.info

Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr
A	05.10.87	—	ERN# 0109	P.T.	BG
B	02-91	1.02.014E	CR9 & CR10 WERE 2 1/2W, 5% ZENER DIODES.	GJ	BG



NOTES:
1) WRITE P/N '7001E9044' AND CURRENT REV. LEVEL ON LABEL.

NOTES: 1. REMOVE & DISCARD R18, R19, CR9 & CR10.

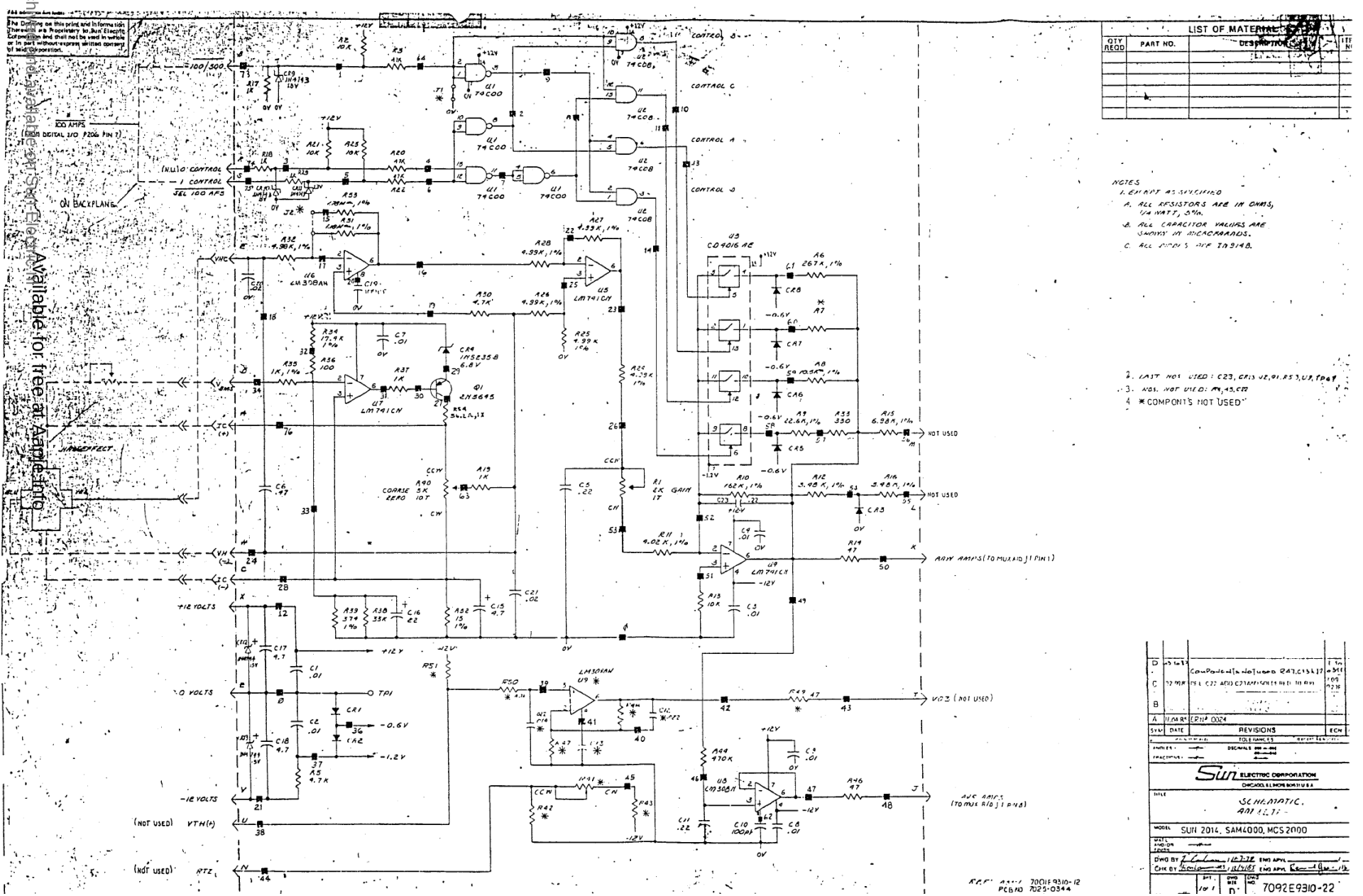
Item	Qty	Dwg Part no	Description	Remarks
4	1	3.0678.563	LABEL IDENT, (7001E9044, Rev A)	
3	2	0803-5001	DIODE, ZENER, 10V, 1W, 2%	CR9, CR10
2	2	3.0680.762	RESISTOR, 120Ω, 5%, 1/2W	R18, R19
1	1	7001-0374	PCB Ass'y VOLT/OHM Rev. "E"	

Scale N.T.S.
Drawn by Tjin A Soe M. 22.10.87
Checked by Peter Tol 11.05.88
Approved Bernard Jan 17.5.88
Remarks SUN 7014, SAM 4000, MCS 2000.
Finish

Unless otherwise specified

Description PRINTED CIRCUIT BOARD Ass'y VOLT/OHM
Dwg no 7001E9044
Sheet 1 of 1
Code
Project no
Iss B

REF. B/M# 0603C/5a
REF. MOD. INSTR.# 0692E9305-69
REF. PCB# 7025-0615
REF. SCHEM# 7092E9023



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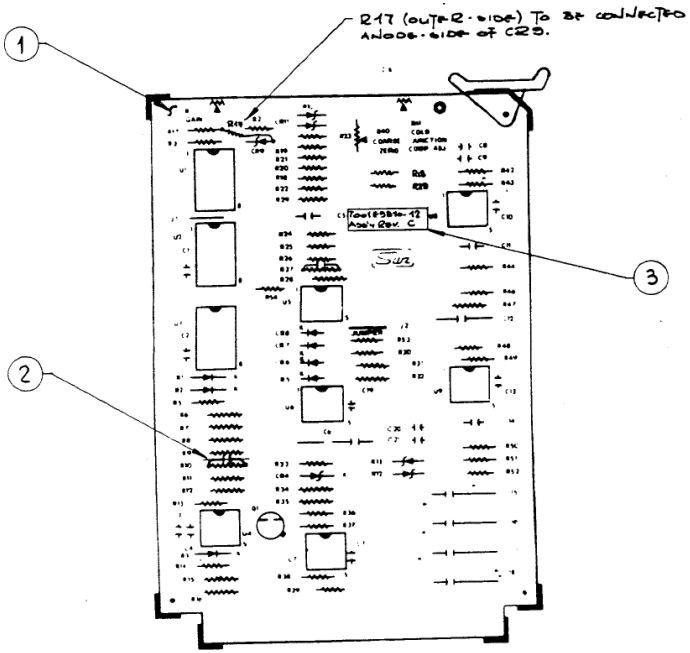
Archive Image Available for Free at Archive.org

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Available for free at Aapje.info

Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr
A	01.0186	6.03.0088	R17 SOLDERED TO THE RIGHT HAND SIDE OF C23. ADD. C22 & SOLDERED ACROSS R27.		
B	02.0887	7.09.025E	DELETED C22. ADDED C23 & SOLDERED ACROSS R10. REVISED & REDRAWN		
C	02.0888	8.05.025E	ADD. REF. B/M # & REF. MOD. INSTR. #	P.T.	BG

COMPONENT-SIDE (LEGEND)



Item	Qty	Dwg Part no	Description
3	1	3.0673.563	LABEL IDENT (700IE9310-12 REV.C)
2	1	3.0679.511	CAPACITOR, 0.22μF, 60VDC, 10%
1	1	700-0222-000	PCB ASS'Y AMMETER/TEMP. REV. 7

N.T.S.

TJIN A SOE M.	02.11.87	SUN 2014, SAM 4000, MCA 2000.
PETER TEL		
BERNARD GEE	17.5.88	

Description: PRINTED CIRCUIT BOARD ASS'Y AMMETER/TEMP.

Dwg no. 700IE9310-12

Sun | A2 | 1 of 1 | C

REF. B/M# 0604C/5G
REF. MOD. INSTR.# 0692E9305-70
REF. PCB# 7025.0344 REV. 7
REF. SCHEM# 7092E9310-22

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LIST OF MATERIAL

QTY REQD	PART NO.	DESCRIPTION	ITEM NO

NOTES:
1. EXCEPT AS SPECIFIED
A) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 5%
B) ALL CAPACITOR VALUES ARE SHOWN IN MICROFARADS.
C) ALL DIODES ARE IN914B
2. UNLESS NOTED OTHERWISE, ALL CAPACITORS ARE 50V

LAST NO'S. USED:
C44, CR27, U14, R108, Q16, IP13

UNUSED

UNUSED

7001E904-5	JUMPER DIODE, IN914B
ASSY #	CR23

REF. PCB # 7025-0429
ASSY # 7001E9045

NOT INSERTED

SEE TABLE

REVISIONS			
A	11-04-82	ECR # 0024	

SUN ELECTRIC CORPORATION
CHICAGO, ILLINOIS 60631 U.S.A.

TITLE: SCHEMATIC TIMING

MODEL: SUN 2014, SAM 4000, MC52000

DWG BY: C. GOODELL 12-27-78 ENG APPL:
CHK BY: [illegible] 12-28-78 ENG APPL:

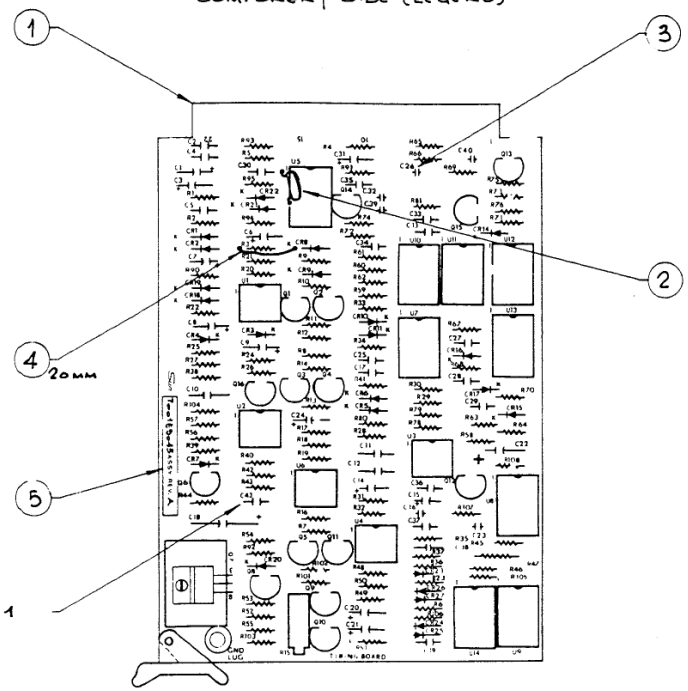
NONE

SIZE D | DWG NO 7092E 9024

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Hole Schedule			Revisions					
Code	Qty	Dia	Sym	Date	ECN	Description	Check	Appr
			A	07.10.87		ERN#0109	G.T.	GB

COMPONENT-SIDE (LEGEND)



NOTES:

1. REMOVE & DISCARD C26 AND C43.

5	1	3.0673.563	LABEL IDENT (7001E9045 Rev.A)	
4	20mm	3.0637.593	WIRE LINK 28 AWG	
3	1	3.0679.643	CAPACITOR 4.7nF, 100V	C26
2	1	3.0679.683	CAPACITOR 33nF, 250V	
1	1	7001-0138-001	PCB Ass'y TIMING Rev. M	
Sym	Qty	Dwg Part No	Description	Remarks

Scale N.T.S.	Date 22.10.87	Assembly SUN 2014, SAM 4000, MCS 2000.	
Drawn Tjin A Soe M.	11.05.88		
Checked Peter Tol	17.5.88		
Approved Bernard Ger			

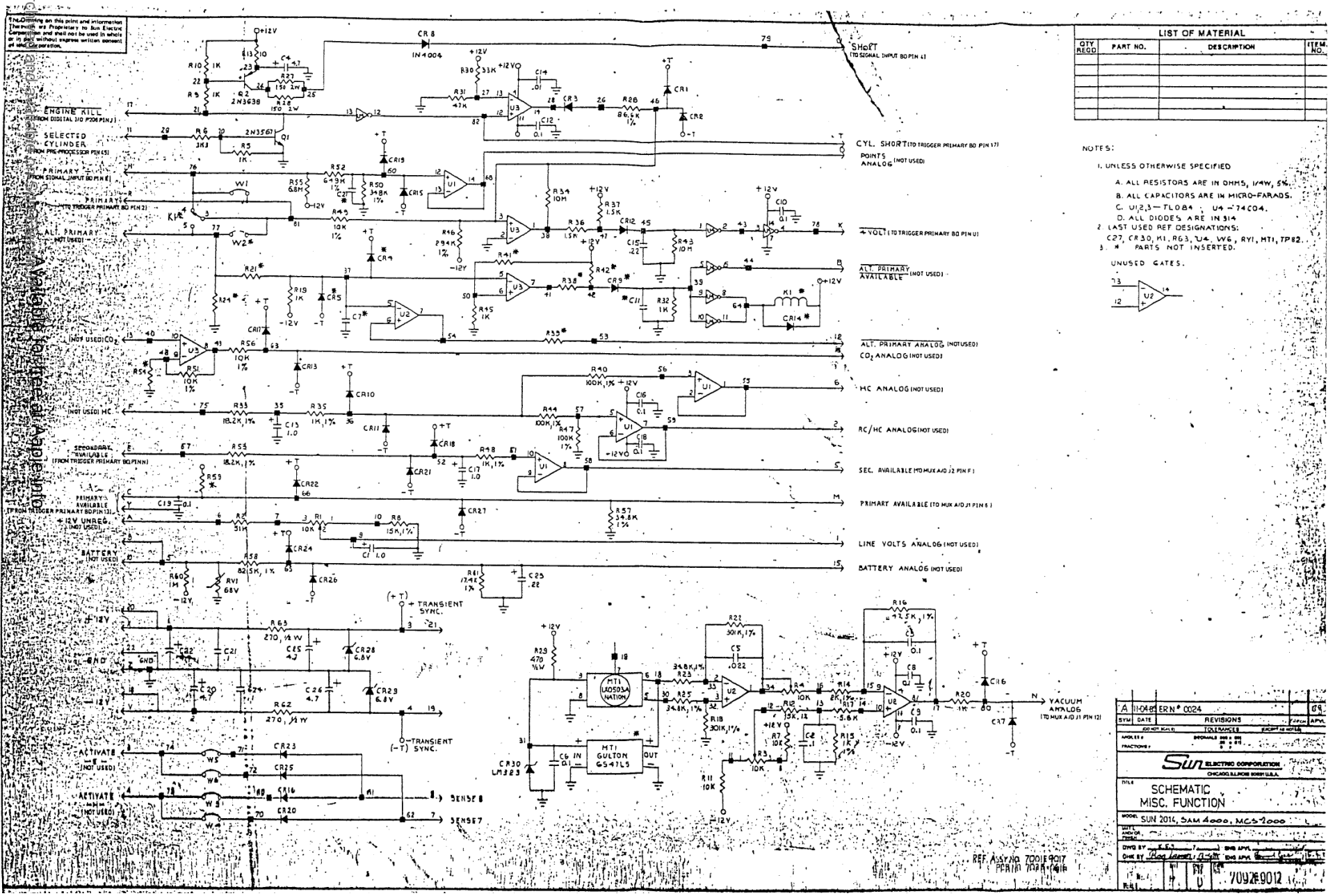
PRINTED CIRCUIT BOARD Ass'y TIMING — 7001E9045

Sun — A2 — 1:1 — Issue A

REF. B/M* 0603C/56
REF. MOD. INSTR.* 0692E9305-71
REF. PCB* 7025-0429 REV. H
REF. SCHEM* 7092E9024

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LIST OF MATERIAL

QTY REQD	PART NO.	DESCRIPTION	ITEM NO.

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   - A. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
   - B. ALL CAPACITORS ARE IN MICRO-FARADS.
   - C. U1,2,3 — TL084 , U4 — 74C04.
   - D. ALL DIODES ARE IN 914
2. LAST USED REF DESIGNATIONS: C27, CR30, K1, R63, U4, W6, RV1, MT1, TP82.
3. * PARTS NOT INSERTED.

UNUSED GATES.

SYM	DATE	REVISIONS	APVD
A	11-04-85	ERN # 0024	GG

Sun ELECTRIC CORPORATION, CHICAGO, ILLINOIS 60631 U.S.A.

TITLE: SCHEMATIC MISC. FUNCTION

MODEL: SUN 2014, SAM 4000, MCS-2000

DWG BY: K.S. DWG APVL:

CHK BY: Bob Lewis 11-4-85 CHG APVL:

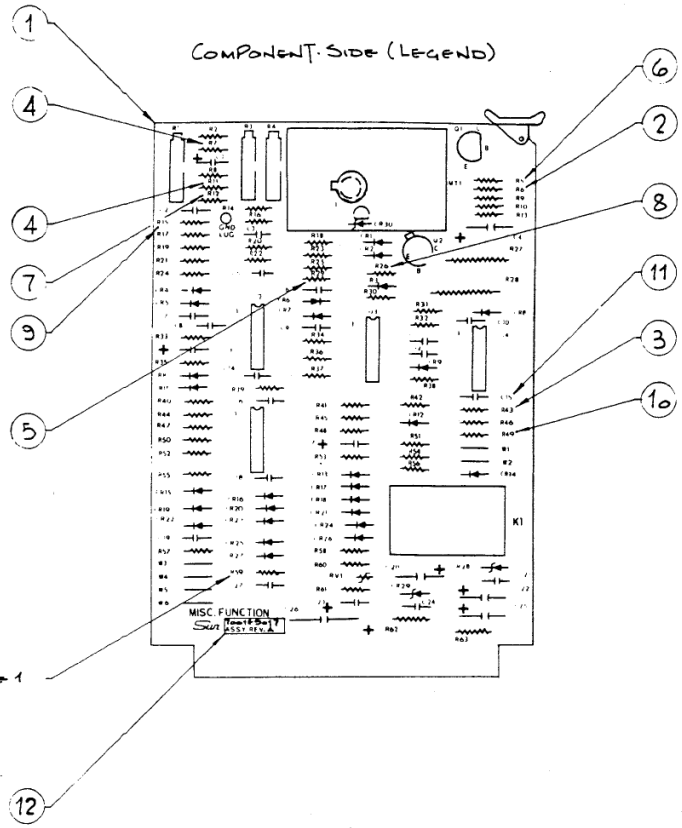
SIZE	DWG NO.	REV
B	700189012	D

SHEET 1 OF 1

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A	27.10.87	ERN* 0109	P.T. BG

COMPONENT SIDE (LEGEND)



NOTES:

1. REMOVE & DISCARD COMPONENTS R5, R6, R7, R11, R12, R15, R26, R29, R43, R49, R59 AND C15.

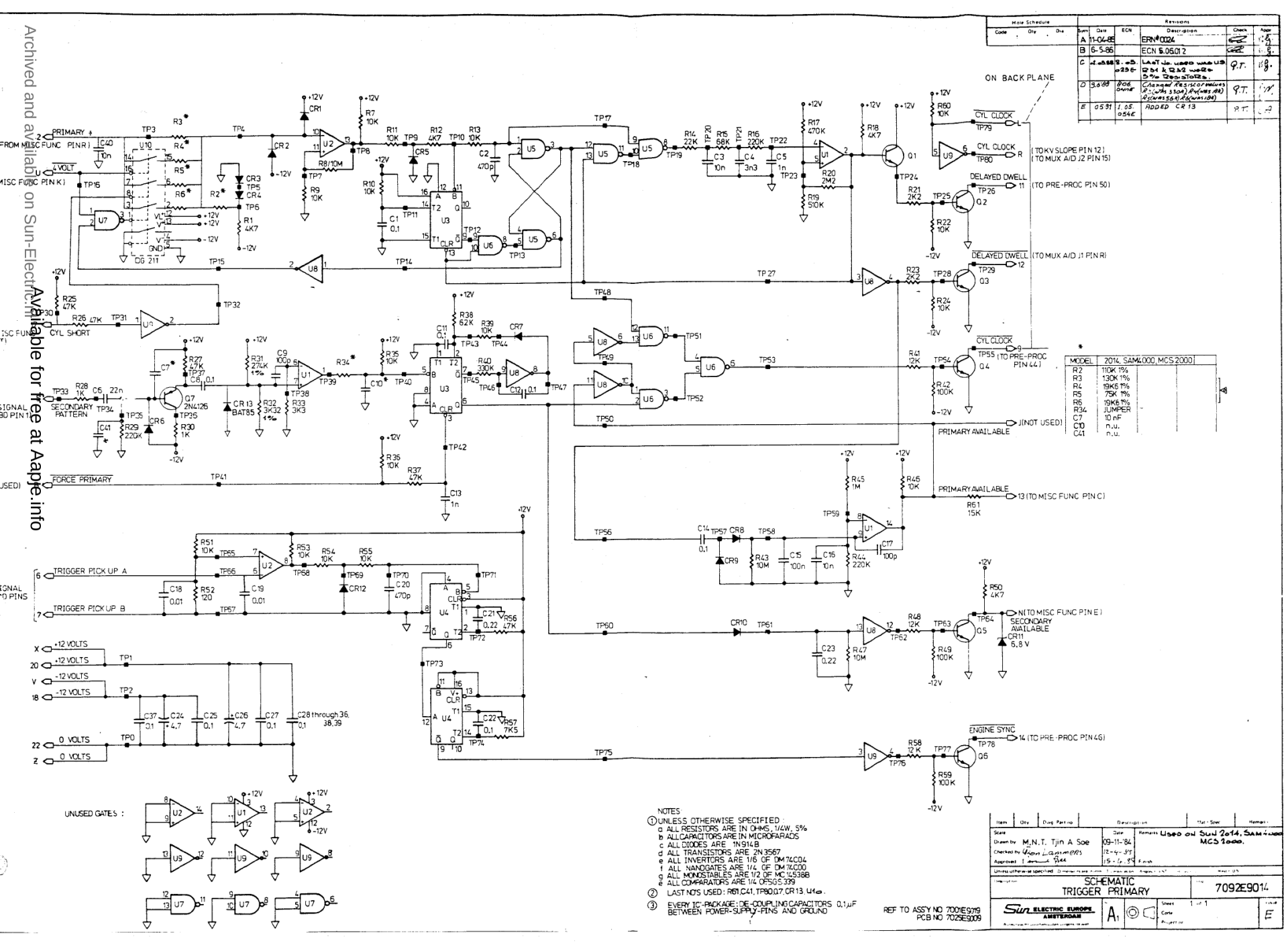
12	1	3.0673.563	LABEL IDENT (7001E9017 Rev A)	
11	1	3.0679.546	CAPACITOR 22nF, 250V, 10%	C15
10	1	1670.1004	RESISTOR 10K, 1%, ¼W	R49
9	1	1670.1003	RESISTOR 1K, 1%, ¼W	R15
8	1	1670.8664	RESISTOR 866Ω, 1%, ¼W	R26
7	1	1670.1504	RESISTOR 15K, 1%, ¼W	R12
6	1	3.0680.642	RESISTOR 1K, 5%, ¼W	R5
5	1	3.0680.728	RESISTOR 470Ω, 5%, ½W	R29
4	2	3.0680.603	RESISTOR 10K, 5%, ¼W	R7, R11
3	1	3.0680.675	RESISTOR 10M, 5%, ¼W	R43
2	1	3.0680.597	RESISTOR 3K3, 5%, ¼W	R6
1	1	7001-0375	PCB ASS'Y MISC. FUNCTION REV J	

N.T.S.	27.10.87	SUN 2014, SAM 4000, MCG 2000
TJIN A SOE M.	11.05.88	
Peter Tol		
Bernard Gee	17.5.88	

REF. B/M* 0606C/5a
REF. MOD. INSTR.* 0692E9305-72
REF. PCB* 7025-0616 REV. G
REF. SCHEM* 7092E9012

PRINTED CIRCUIT BOARD ASS'Y MISC. FUNCTION		7001E9017
Sun	A2	1 1 A

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MODEL	2014, SAM4000, MCS 2000
R2	110K 1%
R3	130K 1%
R4	196K 1%
R5	75K 1%
R6	196K 1%
R34	JUMPER
C7	10 nF
C10	n.u.
C41	n.u.

NOTES
1. UNLESS OTHERWISE SPECIFIED :
   a ALL RESISTORS ARE IN OHMS, 1/4W, 5%
   b ALL CAPACITORS ARE IN MICROFARADS
   c ALL DIODES ARE 1N914B
   d ALL TRANSISTORS ARE 2N3567
   e ALL INVERTORS ARE 1/6 OF DM74C04
   f ALL NANDGATES ARE 1/4 OF DM74C00
   g ALL MONOSTABLES ARE 1/2 OF MC12538B
   h ALL COMPARATORS ARE 1/4 OF SO-339
2. LAST NO'S USED : R61, C41, TP80, Q7, CR13, U4
3. EVERY IC-PACKAGE : DE-COUPLING CAPACITORS 0,1 µF BETWEEN POWER-SUPPLY-PINS AND GROUND

REF TO ASSY NO 7001E9979
PCB NO 7025E9009

Sym	Date	ECN	Description	Check	Appr
A	11-04-85		ERN# 0124		
B	6-5-86		ECN 5.06.012		
C	1.8.88	8.8.0256	Last de. used was U9 R54 k R52 used 5% resistors.	P.T.	
D	9.8.88	806 0008	Changed resistances R1 (2k 3304), R4 (was 4K) R5 (was 56K) R6 (was 10K)	P.T.	
E	05 91	1.05. 054E	ADDED CR 13	P.T.	

Item	Qty	Dwg Part no	Description	Mat'l Spec	Remarks

Scale
Drawn by M.N.T. Tjin A Soe — Date 09-11-84
Checked by Hans Lammers — 12-4-85
Approved J. Lammers — 15-1-85
Finish
Remarks Used on Sun 2014, SAM 4000 MCS 2000.
Unless otherwise specified: Dimensions in mm — Tolerances: Angles ±1° — Surface texture

SCHEMATIC
TRIGGER PRIMARY

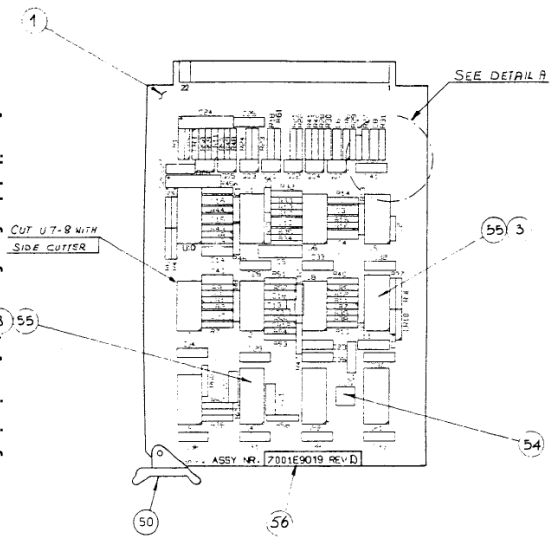
7092E9014

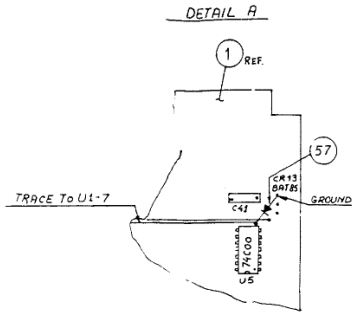
Sun ELECTRIC EUROPE AMSTERDAM

Sheet 1 of 1
Code
Project nr
A1
E

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1	27.6.84	—	PRELIMINARY DRAWING			
A						
B	24.10.87	—	ERN° 0105		P.T.	
C	9.1988	006,0406	Changed R3(WAS 470R VALUES R3(WAS 330R) R4(WAS 68R) R5(WAS 56R) R6(WAS 18R), ADD LABEL.		P.T.	
D	05.91	1.05 0546	ADDED ITEM 57 U7-8 CUT		P.T.	





57	1	7034E30558a	DIODE BAT 85		CR13
56	1	3-a776-563	LABEL ID4 VT		
55	2	3-a776-673	IC SOCKET 16 Pins (used on)		U3, U4
54	1	a536-a3a2a	TERMINAL Post		GND Lug
53	1	a668-a3a1a	JUMPER INSULATED (2x8a o/w R)		R34
52	1	3-a68a-554	RESISTOR, 15kOhm, 5%, 1/4W		R61
51					
50	1	0681-0802-006	CARD EXTRACTOR		
49					
48	1	0003-0680-585	RESISTOR 510kOhm 5% 1/4W		R19
47	1	0003-0680-601	RESISTOR 1MOhm 5% 1/4W		R45
46	1	0003-0680-567	RESISTOR 2M2Ohm 5% 1/4W		R20
45	3	0003-0680-575	RESISTOR 10MOhm 5% 1/4W		R8,43,47
44	1	0003-0680-573	RESISTOR 470kOhm 5% 1/4W		R17
43	2	16** 1[illegible]	RESISTOR 19x6kOhm 1% 1/4W		R4,6
42	1	1670-7504-006	RESISTOR 75kOhm 1% 1/4W		R5
41	1	1670-1105-000	RESISTOR 110kOhm 1% 1/4W		R2
40	1	1670-1305-000	RESISTOR 130kOhm 1% 1/4W		R3
39	1	0003-0680-659	RESISTOR 330kOhm 5% 1/4W		R40
38	1	1670-2705-000	RESISTOR 270kOhm 1% 1/4W		R31
37	3	0003-0680-657	RESISTOR 220kOhm 5% 1/4W		R16, 29,44
36	3	0003-0680-572	RESISTOR 100kOhm 5% 1/4W		R42,49,59
35	1	0003-0680-653	RESISTOR 68kOhm 5% 1/4W		R15
34	1	0680-2098-000	RESISTOR 62kOhm 5% 1/4W		R38
33	5	0003-0680-590	RESISTOR 47kOhm 5% 1/4W		R25,26,27,37,58
32	1	0003-0680-553	RESISTOR 22kOhm 5% 1/4W		R14
31	3	0003-0680-648	RESISTOR 12kOhm 5% 1/4W		R41,48,58
30	16	0003-0680-603	RESISTOR 10kOhm 5% 1/4W		R7,9,11,13,22,24,35,36,39,46,51,53*,55,60,62
29	1	0680-2072-000	RESISTOR 7k50hm 5% 1/4W		R57
28	4	0003-0680-500	RESISTOR 4k70hm 5% 1/4W		R1,12,18,50
27	1	1670-3323-000	RESISTOR 3k32 Ohm 1% 1/4W		R32
26	1	0003-0680-597	RESISTOR 3k3 Ohm 5% 1/4W		R33
25	2	0003-0680-589	RESISTOR 2k2 Ohm 5% 1/4W		R21,23
24	2	0003-0680-642	RESISTOR 1kOhm 5% 1/4W		R28,30

22	2	0860-0112-000	CAPACITOR ceramic 0.1µF 50V		C25,27
21	2	0860-0097-000	CAPACITOR ceramic 0.01µF 100V 20%		C7,19
20	2	0860-0056-000	CAPACITOR mica 100pF 500V		C9,17
19	2	0003-0679-631	CAPACITOR ceramic 470pF 1000V		C2,20
18	1	0860-0007-000	CAPACITOR ceramic 0.001µF 500V		C13
17	2	0679-1329-000	CAPACITOR met poly 0.22µF 100V		C21,23
16	17	0003-0679-563	CAPACITOR met poly 0.1µF 100V		C1,8,11,12,14,15,22,C28-31
15	1	0003-0679-653	CAPACITOR met poly 0.022µF 100V		C6
14	4	0679-1312-000	CAPACITOR met poly 0.01µF 100V		C3,16,18,40
13	1	0003-0679-715	CAPACITOR met poly 0.0033µF 100V		C4
12	1	0003-0679-684	CAPACITOR poly film 0.001µF 100V		C5
11	2	0693-0513-000	CAPACITOR electrolytic 47µF 16V		C24,26
10	1	9405235-000	DIODE ZENER 5.8V 1/2W		CR11
9	11	0771-0272-000	DIODE 1N914 B		CR1-10,12
8	1	0003-0776-556	TRANSISTOR 2N4126		Q7
7	6	0776-0151-000	TRANSISTOR 2N3567		Q1-6
6	1	0003-0776-656	INTEGRATED CIRCUIT DG211CJ		U10
5	2	0003-0776-534	INTEGRATED CIRCUIT DM74C04		U6,U9
4	3	0003-0776-533	INTEGRATED CIRCUIT DM74C00		U8,U10,U7
3	2	0003-0776-630	INTEGRATED CIRCUIT MC14538B		U5,U12
2	2	0003-0776-678	INTEGRATED CIRCUIT SOS 339		U11,U12
1	1	7025E9009-000	TRIGGER PRIMARY P.C.B.		

Used on Sun 2014, 2414 too MCS 2000.

F BRUGMAN	07-05-86	
Peter Tol	11.05.88	
Bernard Jan	17.5.88	

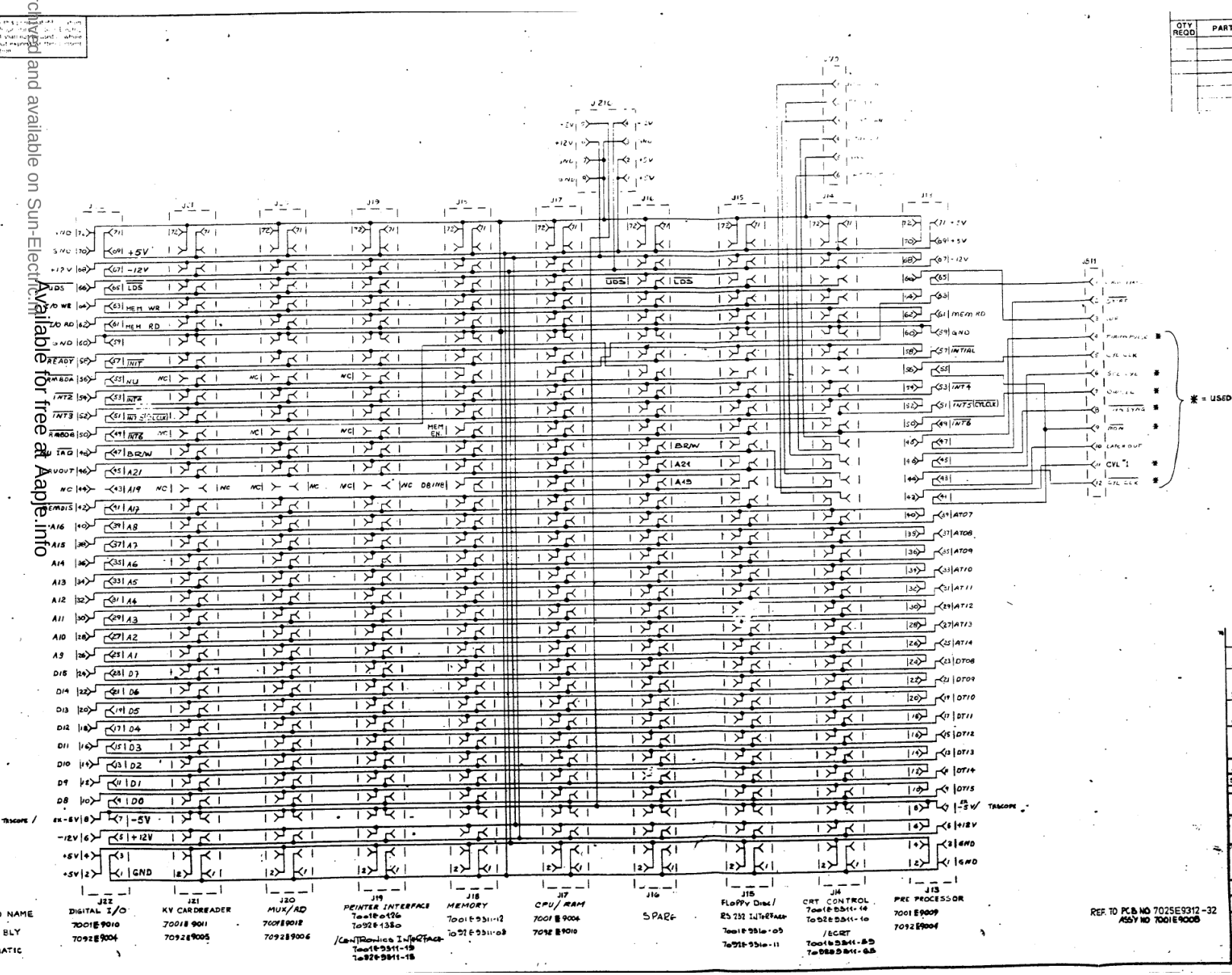
Ref. B/M° 0611C/5a

REFER TO P.C.B. DRAWING 7025E9009-000
REFER TO SCHEMATIC 7092E9014-000

P.C.B. Assy. TRIGGER PRIMARY BOARD | 7001E9019-000

Sun

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QTY REQD	PART NO.	DESCRIPTION	ITEM NO

SYM	DATE	REVISIONS
E	06-30	ECN 1.03.039 E REF TO PCB WAS 7025-8614
D	[illegible]	ECN # 5.05.0416 ADD. CONTR. INTERFACE FOR J19 DELETED TEST W.C. AT J14 P.J# 46 WERE NOT CONNECTED
C	10-6-86	ECN # 5.05.0256 ADD. CONTR. INTERFACE FOR J19 DELETED TEST W.C. AT J14 P.J# 46
B	21 OCT 85	ECN # 7.85.0068 EXPAND A17 & A21 ADDRESS LINES TO CONNECTOR J14 (CRT CONTROL BD) ECN#1.3.0 WAS SPARE & J16 WAS MEMBD
A	11-04-85	ERN# 0024

DO NOT SCALE — TOLERANCES EXCEPT AS NOTED
ANGLES ± — DECIMALS .000 = .010, .00 = .030, .0 = .060
FRACTIONS ± — 0 = 1/64

SUN ELECTRIC CORPORATION CHICAGO, ILLINOIS 60656 U.S.A.

TITLE: SCHEMATIC DIGITAL BACKPLANE

MODEL: SUN 2014, SAM 4000, MCS 2000, etc. 2x0

DRAFTING SUPERVISOR — CHECKED

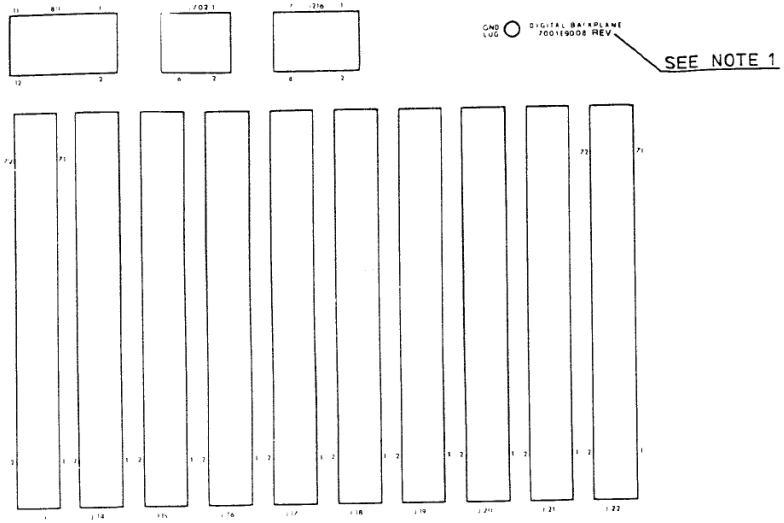
DWG BY Bob 12-2-85 ENG APPR.

CHK BY Wm Lawrence 12-4-85 ENG APPR.

SCALE — SHT 1 OF 1 — DWG SIZE D — DWG NO. 7092E9002

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Revisions					
Rev	Date	ECN	Description	Check	Appr
F	06-'91	1.03. 034E	INTEGRATED HDD'S IN NEW COPPER. ADDED COMPONENTS LIST.	Ø	CA



KEYING CHART		
CONNECTOR DESIGNATION	BETWEEN PINS	BETWEEN PINS
J13	5-7	63-65
J14	5-7	61-63
J15	11-13	51-53
J16	3-5	51-53
J17	9-11	59-61
J18	5-7	51-53
J19	—	—
J20	5-7	59-61
J21	—	—
J22	5-7	57-59

NOTES:
1) WRITE CURRENT REV. LEVEL

LINE NR	DIRECT ASSEM PART NR	QUAN.	COMPONENTS & SUB ASSEMBLIES	B/M PAGE NR ITEM NR.
1	7025E9312-32	1	PCB DIGITAL BACKPLANE	
2	4162-0370	10	CONNECTOR 72 PIN (J13-22)	
3	4162-0337	1	CONNECTOR 12 PIN (J811)	
4	4162-0328	1	CONNECTOR 8 PIN (J216)	
5	4162-0327	1	CONNECTOR 6 PIN (J702)	
6	0536-0302	1	TERMINAL POST (GND LUG)	
7	0610-0147	20	SCREW	
8	7031-0153-05	2	INSULATOR STRIP	
9	0722-0522-09	2	SUPPORT CHANNEL	
10	4162-0913	16	KEY CONNECTOR	

REF PCB 7025E9312-32
REF SCHEM 7092E9002

Item | Qty. | Dwg. Part No. | Description | Remarks

Designed by
Drawn by R. v.d. HOEF 24-06-91
Checked by O. Brunon 1/07/91
Approved Austroni 2/7-91

Sheet: SUN 2014, SAM 4000, MCS 2000, OCS 2000.
Material
Finish

Unless otherwise specified: Dimensions are in inches and fractions. Angles ± Tolerances on machined surfaces ± Surface finish

PRINTED CIRCUIT BOARD ASS'Y
DIGITAL BACKPLANE

Dwg. No. 7001E9008

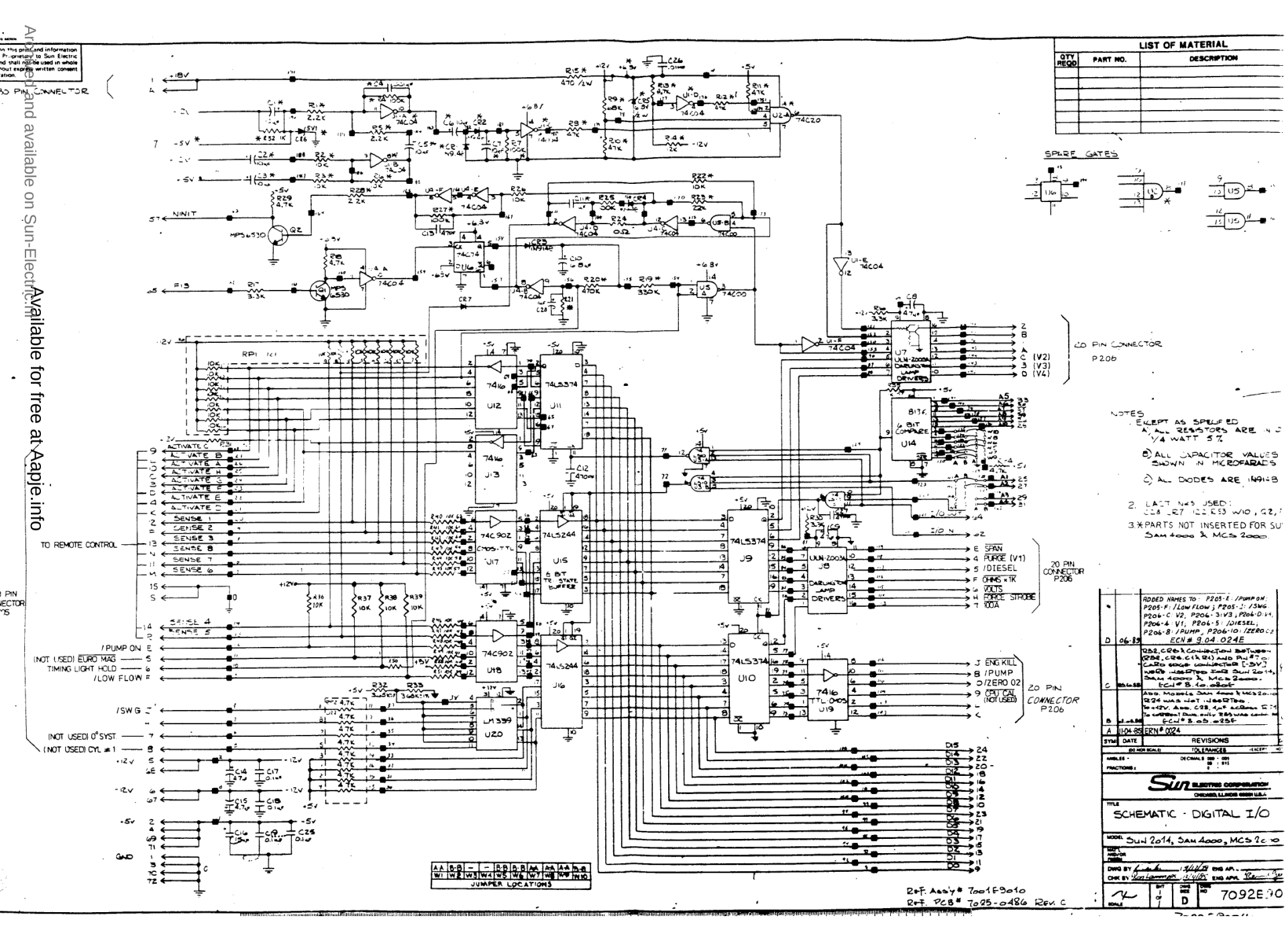
Sun

A2

Sheet 1 of 1
Scale
Project No. 0007

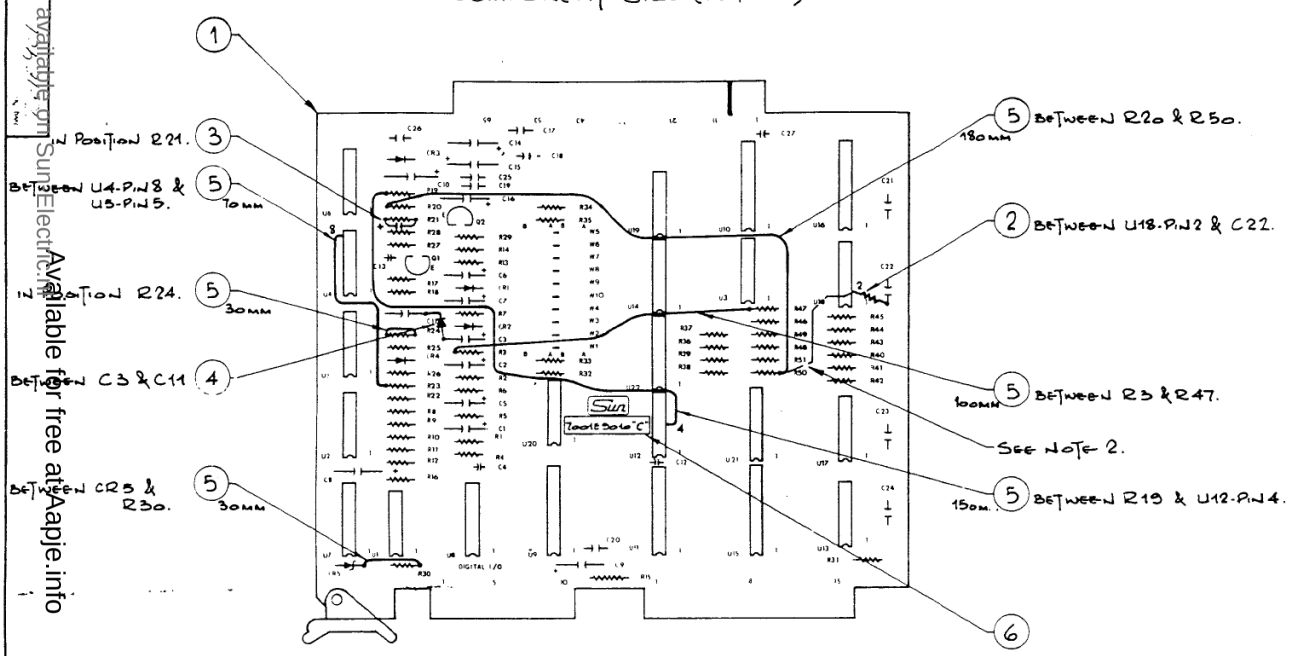
Rev F

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COMPONENT-SIDE (LEGEND)



Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr
A	5.10.87		ERN# 0109	P.T.	BB
B	31.08.88	808066	ADDED R27, R28 TO NOTE 1; CHANGED MOUNT. DESCR. IT 2.	P.T.	
C	25.6.88	B.10.0806	DELETED RESISTOR R52 WAS IN PARALLEL WITH C1. DELETED DIODE CR6 WAS CONN. BETWEEN R4 (A) & R10 (K). DELETED JUMPER WIRE BETWEEN PIN# 7 OF CARD EDGE CONN. & C1 (+)	P.T.	BB

NOTES: 1. REMOVE & DISCARD R15, R19 THROUGH R24, R27, R28, R52 (POSITIONED IN PARALLEL WITH C10), C11, CR5, CR6 (POSITIONED BETWEEN R1 & R10) & LINK WIRE (POSITIONED BETWEEN C1 & CARD EDGE CONNECTOR).

2. CUT TRACK BETWEEN R50 OUTER-SIDE & U18 PIN# 2, AS SHOWN.

JUMPER LOCATIONS			
MODEL	SUN 2014	SAM 4000	MCS 2000
ASS'Y NO.	7001E9010	7001E9010	7001E9010
W1	A-A	A-A	A-A
W2	B-B	B-B	B-B
W3	NOT USED	NOT USED	NOT USED
W4	NOT USED	NOT USED	NOT USED
W5	B-B	B-B	B-B
W6	B-B	B-B	B-B
W7	A-A	A-A	A-A
W8	A-A	A-A	A-A
W9	A-A	A-A	A-A

REF. B/M# 0609C/SG.
REF. MOD. INSTR.# 0692E9305-76
REF. PCB# 7025-0486 REV. C

Item	Qty	Dwg. Part no.	Description	Remarks
6	1	3.0673.563	LABEL IDENT (7001E9010 Rev C)	
5	560MM	3.0637.655	WIRE LINK, 24 AWG, BLACK	
4	1	0771.0272	DIODE, 1N 914 B, 75V, 100 mA.	
3	1	3.0679.702	CAPACITOR, 1mF, 63V	
2	1	0680.2075	RESISTOR, 10K, 5%, 1/4W	
1	1	7001-0389	PCB ASS'Y DIGITAL I/O REV. C	

Scale N.T.S.
Drawn by TJIN A SOE M. — Date 21.10.87
Checked by Peter Tel — 11.05.88
Approved Bernard Gac — 17.5.88
Remarks SUN 2014, SAM 4000, MCS 2000.
Finish

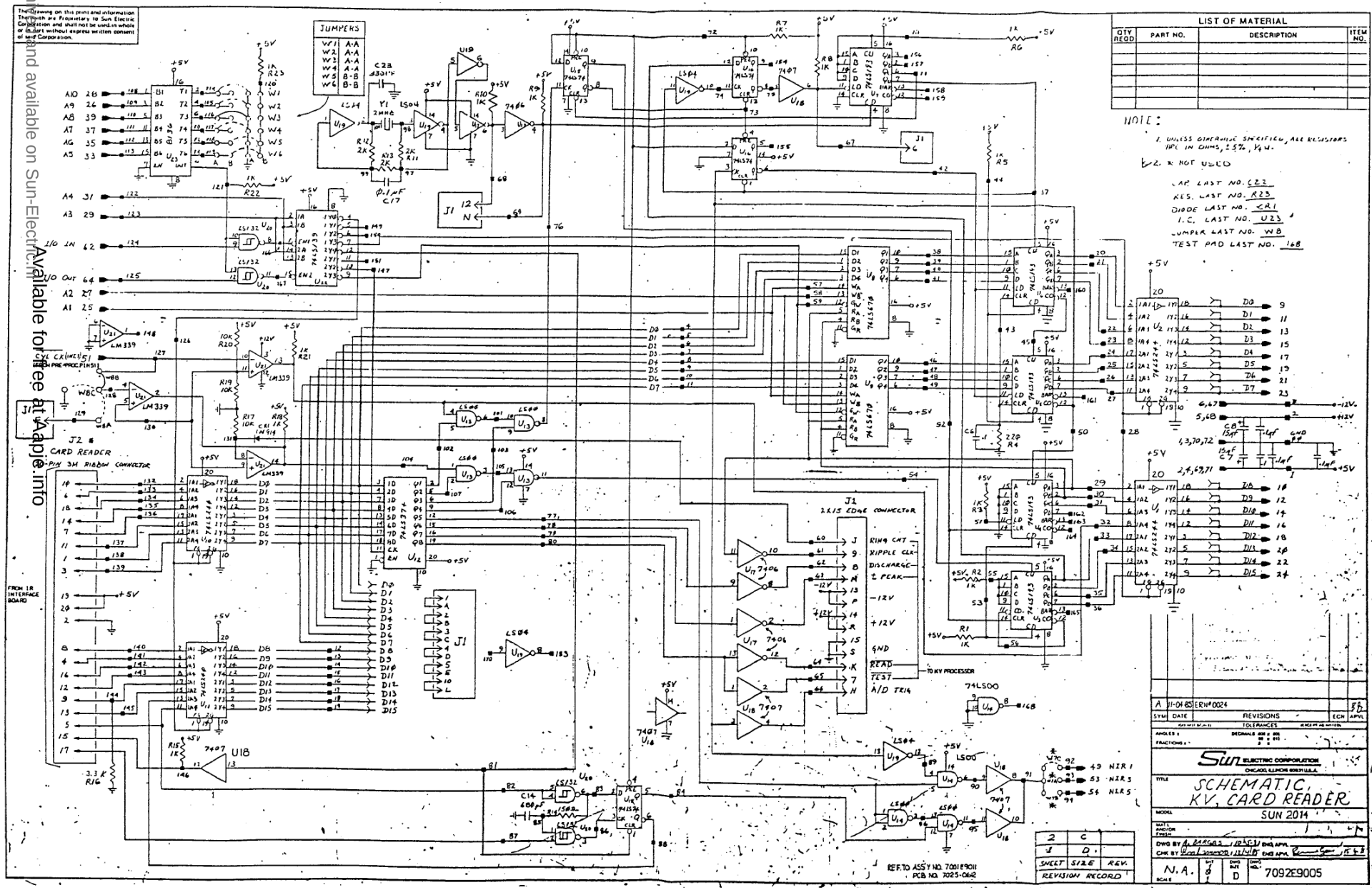
Unless otherwise specified: Dimensions are in mm; Tolerances on: Angles ± 0.5°, Holes ± 0.1, Rest ± 0.5

Description PRINTED CIRCUIT BOARD ASS'Y DIGITAL I/O
Dwg no. 7001E9010

Sun
A2
Sheet 1 of 1
Code
Project no.
Issue C

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LIST OF MATERIAL

QTY REQD	PART NO.	DESCRIPTION	ITEM NO.

NOTE:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS, ±5%, ¼ W.
2. * NOT USED

CAP. LAST NO. C22
RES. LAST NO. R23
DIODE LAST NO. CR1
I.C. LAST NO. U23
JUMPER LAST NO. W6
TEST PAD LAST NO. 168

SYM	DATE	REVISIONS	ECN	APVL
A	11-01-85	ERN# 0024		SD

TOLERANCES

ANGLES ±
FRACTIONS ±
DECIMALS .XX ± .01
.XXX ± .005

Sun ELECTRIC CORPORATION
CHICAGO, ILLINOIS 60631 U.S.A.

TITLE: SCHEMATIC, KV, CARD READER

MODEL: SUN 2014

MATL AND/OR FINISH

DWG BY: A. BARGAS 10/25/85 ENG APVL

CHK BY: [illegible] 12/4/85 ENG APVL

SHEET	SIZE	REV.
N.A.	D	

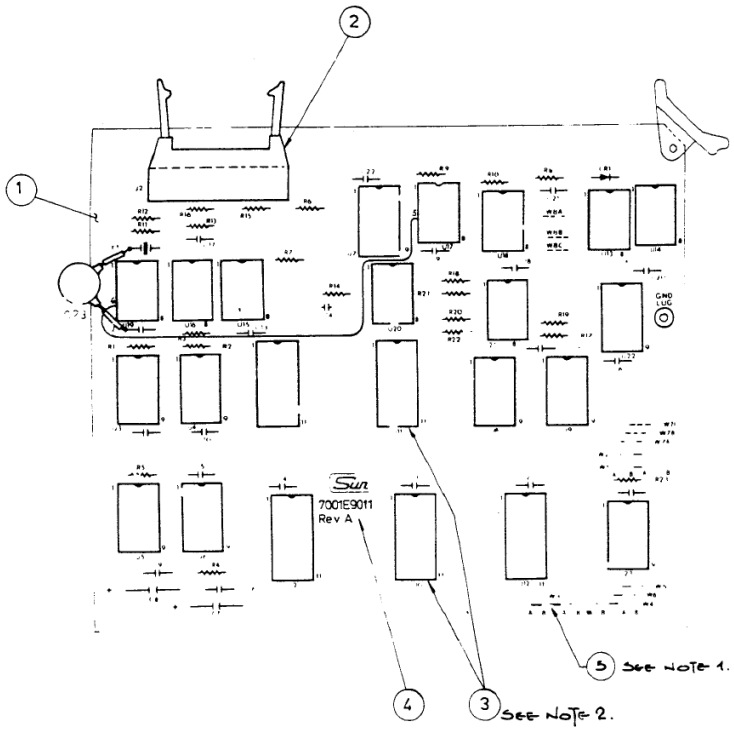
REVISION RECORD

DWG NO. 7092E9005

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Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr
A	07.10.87	—	ERN#0109	P.T.	BG



NOTES:

1. REMOVE JUMPER WIRE W3 FROM POS'N B-B & INSTALL RESISTOR ZERO OHM (ITEM 5) IN POS'N A-A.
2. WHEN NOT PRESENT INSTALL IC's, 74LS240 (ITEM 3) IN POSITIONS U10 & U11.

Item	Qty	Dwg. Part no	Description	Remarks
5	1	0668.0361.000	RESISTOR ZERO OHM.	
4	1	3-0673-563	LABEL SELF-ADHESIVE	
3	2	0773-7240	INTEGRATED CIRCUIT, 74LS240	U10, U11
2	1	3-3931-926	SHROUDED 20 WAY PIN HEADER	J2
1	1	7001-0371	P.C.B. CARD READER/KV CCA Rev "D"	

Scale 1:1
Drawn by H.v/d NIEUWENDIJK — Date 14.10.87
Checked by Peter Tol — 11.05.88
Approved Bernard Lee — 17.5.88
Remarks USED IN Sun 2014, Sun 4000 Mcs 2000.
Finish
Unless otherwise specified: Dimensions are in mm. Tolerances: Angles ± 1°, Machined ± 0.5

PRINTED CIRCUIT BOARD ASSY
CARD READER / KV CCA

Dwg no 7001E9011

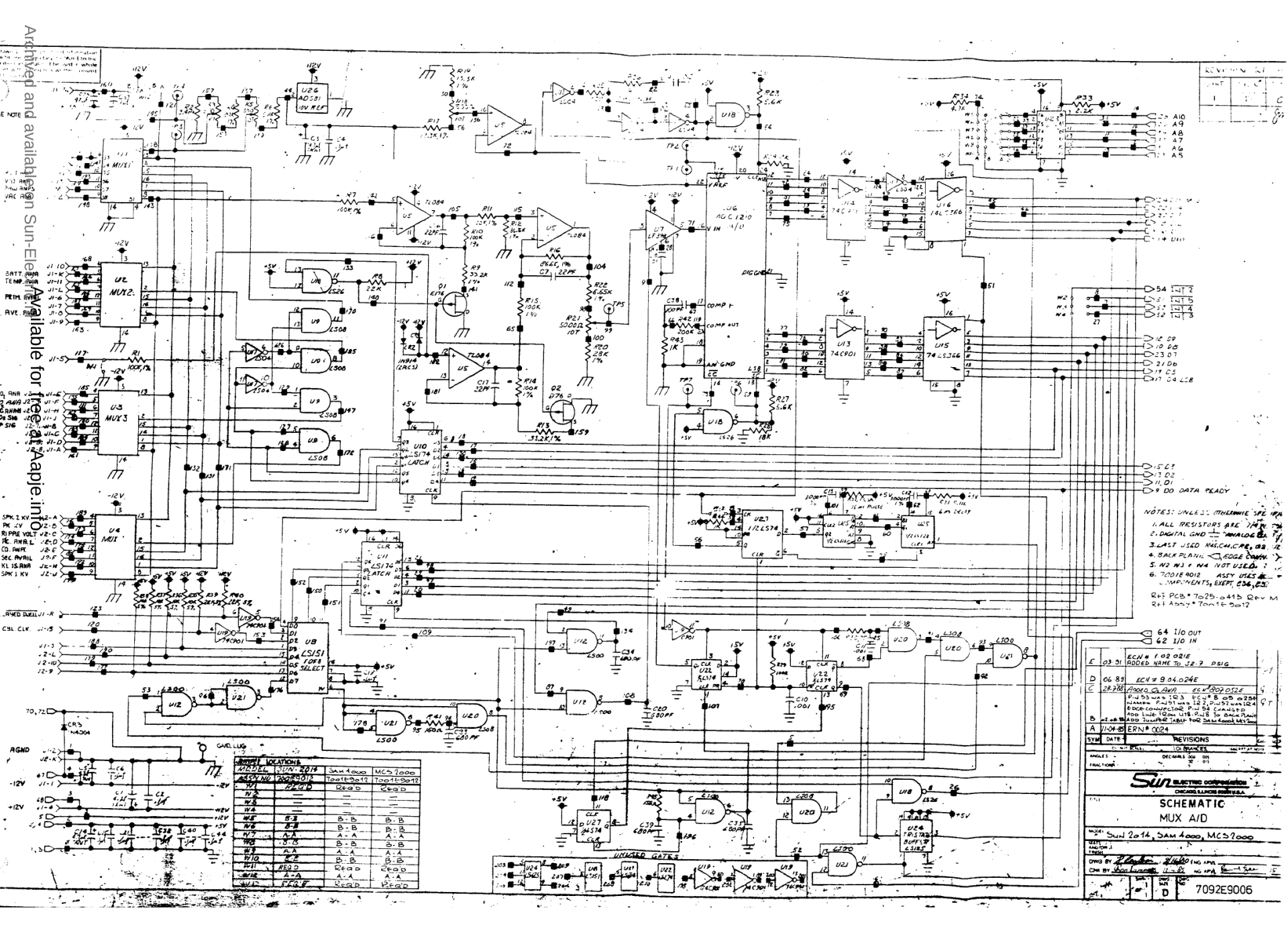
Sun

A2

Sheet 1 of 1
Code
Project no

Issue A

Ref. B/M# 0601C/Sa
Ref. Mod. Instr.# 0692E9305-67
REF. SCHEMATIC DWG. 7092E9005
Ref. PCB# 7025-0612 Rev. A

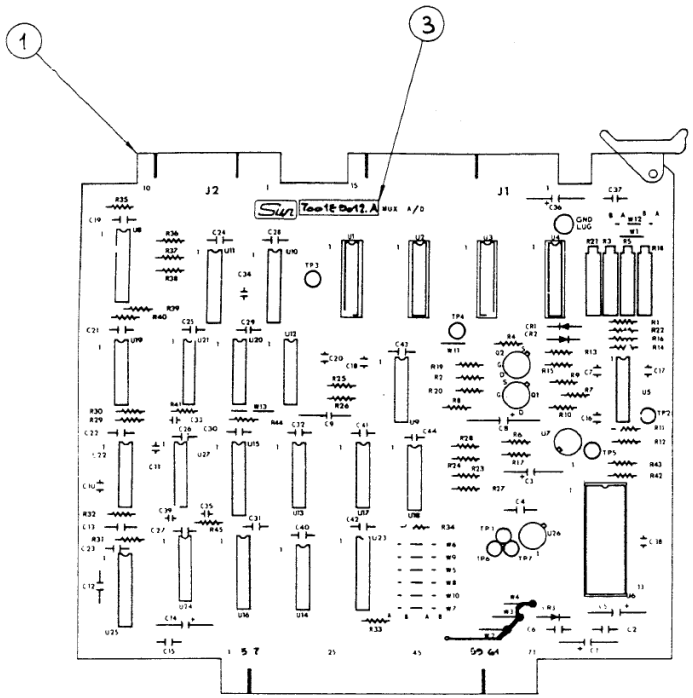


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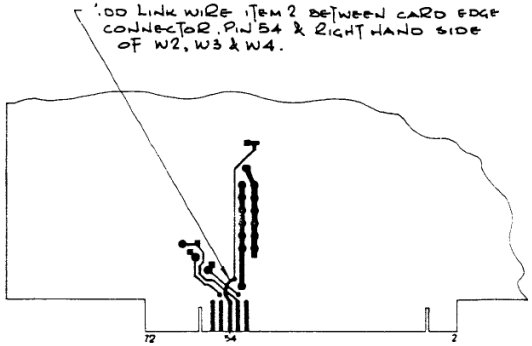
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Available for free at Aapje.info

Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr
A	07.10.87	—	ERN# 0109	P.T.	BG



COMPONENT-SIDE (LEGEND)



SOLDER-SIDE

NOTES: 1. USE REF. DESIGNATIONS & LEGEND FOR LOCATIONS OF COMPONENTS.

2. W13 TO BE INSTALLED AFTER TEST.

JUMPER TABLE	
REF. DESIG.	LOCATION
W1	REQ'D
W2	—
W3	—
W4	—
W5	B-B
W6	B-B
W7	A-A
W8	B-B
W9	A-A
W10	B-B
W11	REQ'D
W12	A-A
W13	REQ'D

SEE NOTE 2

3	1	3.0673.563	LABEL IDENT (7001E-9012. REV.A)
2	20MM	3.0637.593	WIRE LINK 28 AWG
1	1	7001-0122-03	PCB Ass'y MUX A/D Rev. H

N.T.S.	20.10.87	SUN 2014, SAM 4000, MCS 2000.
TJIN A SOE M.	11.05.88	
Galen Tel	17.5.88	
Bernard Lee		

PRINTED CIRCUIT BOARD ASS'Y MUX A/D — 7001E-9012

Sun — A2 — 1 · 1 — A

REF. B/M# 0602C/5G
REF. MOD. INSTR.# 0692E9305.68
REF. SCHEM.# 7092E9006
REF. PCB# 7025-0413 REV.M

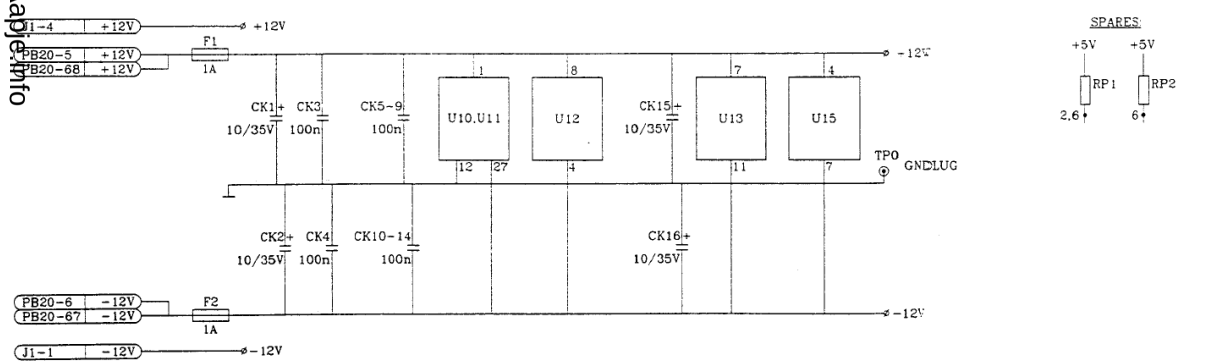
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Rev	Description	By
A	03'94 ERN 1124 R F P	P T
B	05'95 ECN 5.05.055E C11, C20, C45, C46 & C49 REPLACED BY In Was 100n	O.B

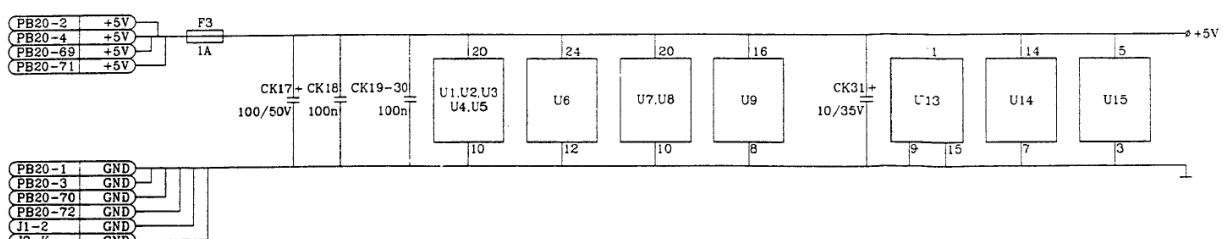
PB20 CONNECTOR			
PIN NO	SIGNAL	PIN NO	SIGNAL
1	GND	37	BA7
2	+5V	38	N.C.
3	GND	39	BA8
4	+5V	40	N.C.
5	+12V	41	N.C.
6	-12V	42	N.C.
7	N.C.	43	N.C.
8	N.C.	44	N.C.
9	BD0	45	N.C.
10	BD8	46	N.C.
11	BD1	47	N.C.
12	BD9	48	CLK 4M
13	BD2	49	N.C.
14	BD10	50	N.C.
15	BD3	51	/INT5
16	BD11	52	/INT3
17	BD4	53	/INT4
18	BD12	54	/INT2
19	BD5	55	N.C.
20	BD13	56	N.C.
21	BD6	57	/INIT
22	BD14	58	N.C.
23	BD7	59	N.C.
24	BD15	60	N.C.
25	N.C.	61	N.C.
26	BA9	62	IORD
27	N.C.	63	N.C.
28	BA10	64	IOWR
29	N.C.	65	N.C.
30	N.C.	66	N.C.
31	N.C.	67	-12V
32	N.C.	68	+12V
33	BA5	69	+5V
34	N.C.	70	GND
35	BA6	71	+5V
36	N.C.	72	GND

J1 CONNECTOR			
PIN NO	SIGNAL	PIN NO	SIGNAL
1	-12V	A	CHANNEL 24
2	GND	B	P SIG
3	N.C.	C	VACU
4	+12V	D	ATEMP
5	N.C.	E	CO2 ANA
6	PRIM AVAIL	F	O2 ANA
7	CHANNEL 14	H	HC ANAH
8	AVE AMP	J	O2 SIG
9	CHANNEL 16	K	BATT ANA
10	CHANNEL 9	L	CHANNEL 12
11	TEMP ANA	M	RAW AMPS
12	VAC ANA	N	KL1 ANA
13	V/Q ANA	P	N.C.
14	CHANNEL 4	R	/DELAYED DWELL
15	CYL CLOCK	S	TRIGGER 4

J2 CONNECTOR			
PIN NO	SIGNAL	PIN NO	SIGNAL
1	O2 SIG	A	SPK 2kV
2	HC ANAH	B	PK 5V
3	O2 ANA	C	RIPPLE VOLT
4	CO2 ANA	D	HC ANA L
5	ATEMP	E	CO ANA
6	VACU	F	SEC AVAIL
7	P SIG	H	KL1E ANA
8	CHANNEL 24	J	SPK 1 kV
9	TRIGGER 7	K	GND
10	TRIGGER 6	L	TRIGGER 5



SPARES:



NOTES:

1) UNLESS OTHERWISE SPECIFIED
   A) ALL RESISTORS ARE IN OHMS.1/4W.1%
   B) ALL CAPACITORS ARE IN MICRO-FARADS
   C) ALL DIODES ARE 1N914 OR 1N4148
   D) ALL IC'S ARE 74HCT-SERIES TYPE
   E) ALL POLARIZED CAPACITORS ARE 16V
2) LAST USED NO'S: R49, RV28, C49, U15, F3, CK31, W3, TP3.
3) NOT USED NO'S: C3-C10, RV3-RV26.
4) COMPONENTS MARKED WITH ■ ARE NOT INSTALLED
5) JUMPER SETTINGS
   W1: A INSTALLED
   B NOT INSTALLED
   C NOT INSTALLED
   W2: A INSTALLED
   B NOT INSTALLED
   W3: A DEFAULT IN COPPER
   B NOT INSTALLED
   C NOT INSTALLED
   D NOT INSTALLED
6) CAPACITORS MARKED WITH • ARE 100nF

Item	Qty	Dwg/Part No	Description	Remarks
Scale	N.T.S.		Date	Used in MCS, OCS
Designed by	KEES STAM		01-94	Material
Drawn by	R. V/D HOEF		03-94	
Checked by	PETER TEL		03-94	
Approved	BERNARD GEE		03-94	Finish

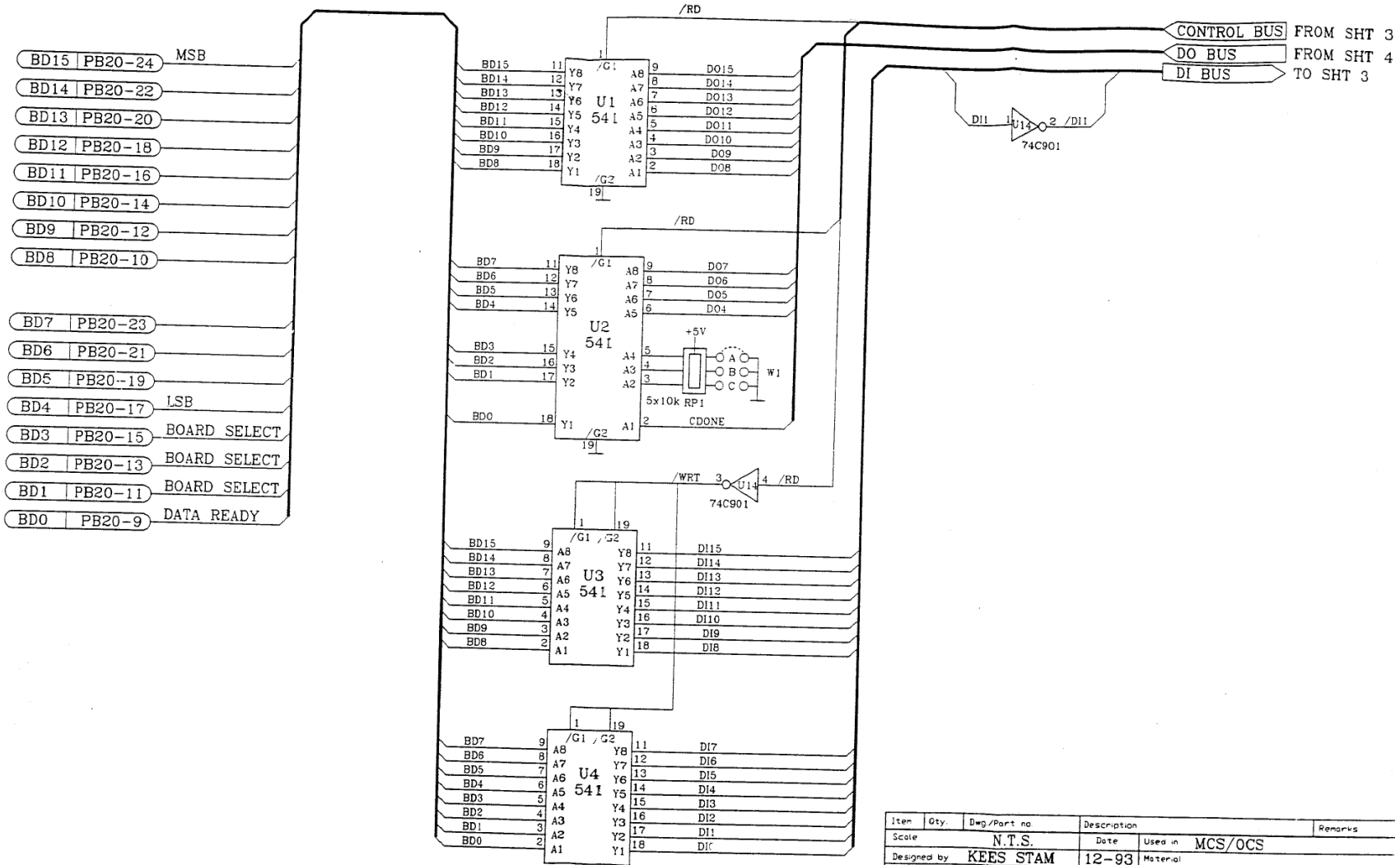
Unless otherwise specified: Dimensions are in mm. Tolerances on: Angles ±5' Holes ±0.1 Rest ±0.5
Remove all sharp corners and remove burrs

Description	Dwg no.
SCHEMATIC MUX ADC BOARD	7092E9313-27

SUN ELECTRIC EUROPE B.V. | A1 | Sheet 1 of 4 | Project no | Rev. B

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Item	Qty.	Dwg./Part no	Description		Remarks
Scale	N.T.S.		Date	Used in	MCS/OCS
Designed by	KEES STAM		12-93	Material	
Drawn by	R. V/D HOEF		12-93		
Checked by	PETER TEL		03-94		
Approved	BERNARD GEE		03-94	Finish	

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±0.1 Rest ±0.5

Remove all sharp corners and remove burrs

Description: SCHEMATIC MUX ADC BOARD

Dwg.no: 7092E9313-27

SUN ELECTRIC EUROPE B.V.

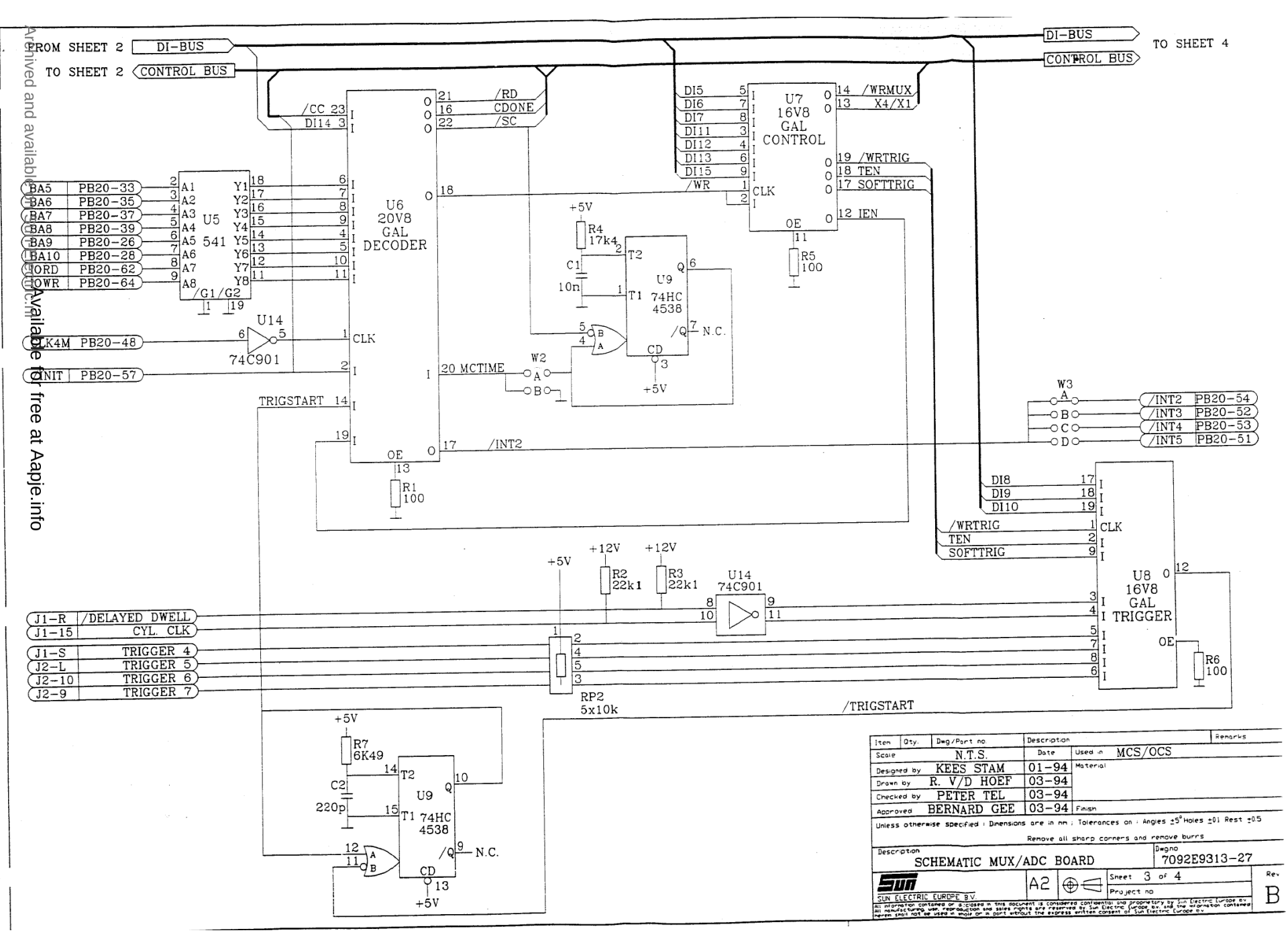
A2

Sheet 2 of 4

Project no

Re: B

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Item	Qty.	Dwg/Part no	Description	Remarks
Scale	N.T.S.		Date	Used in MCS/OCS
Designed by	KEES STAM		01-94	Material
Drawn by	R. V/D HOEF		03-94	
Checked by	PETER TEL		03-94	
Approved	BERNARD GEE		03-94	Finish

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±01 Rest ±05

Remove all sharp corners and remove burrs

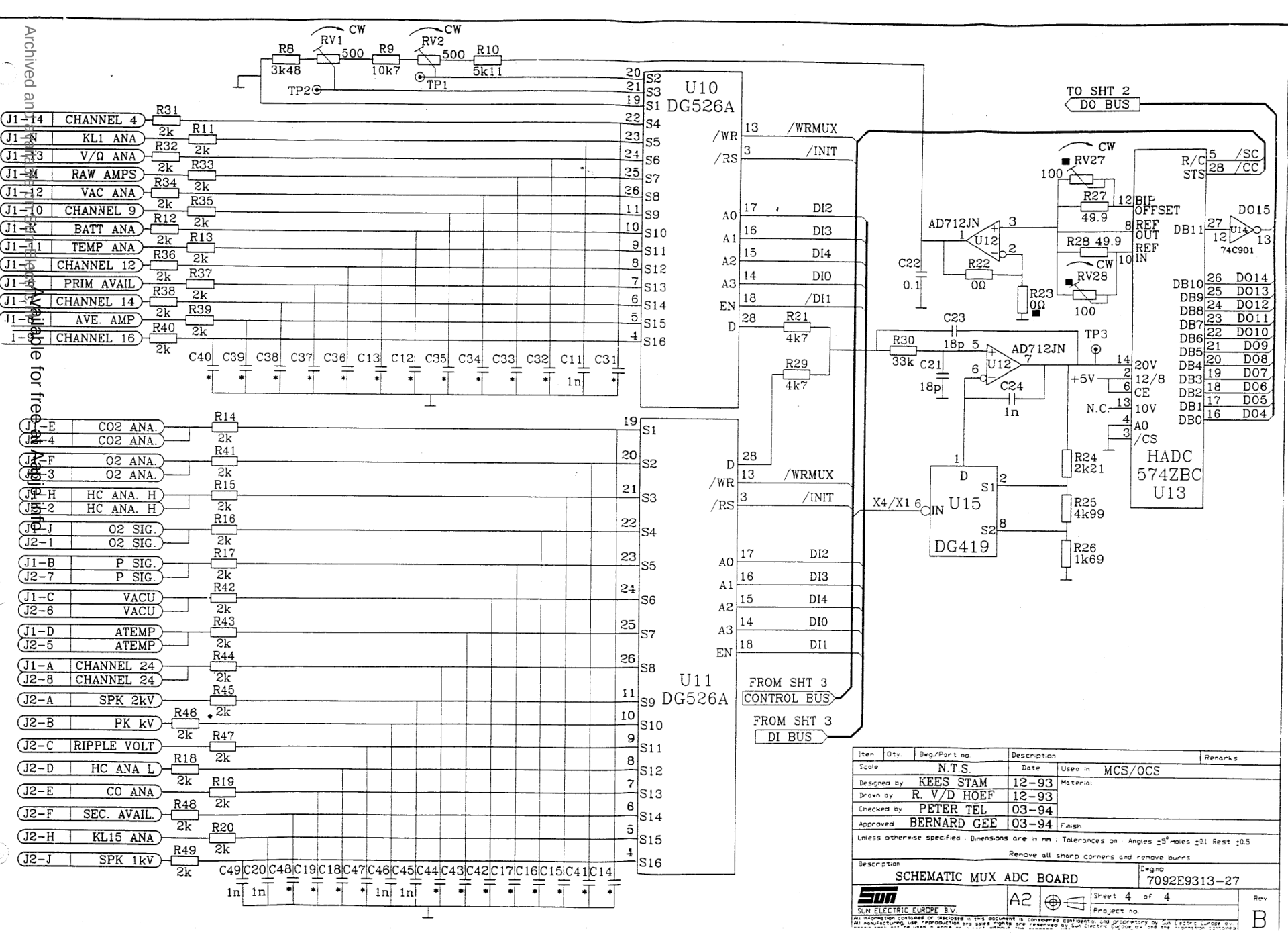
Description	Dwgno
SCHEMATIC MUX/ADC BOARD	7092E9313-27

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Item	Qty.	Dwg/Part no	Description	Remarks
Scale	N.T.S.	Date	Used in MCS/OCS	
Designed by	KEES STAM	12-93	Material	
Drawn by	R. V/D HOEF	12-93		
Checked by	PETER TEL	03-94		
Approved	BERNARD GEE	03-94	Finish	

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±.01 Rest ±0.5

Remove all sharp corners and remove burrs

Description: SCHEMATIC MUX ADC BOARD

Dwgno: 7092E9313-27

SUN ELECTRIC EUROPE B.V.

A2

Sheet 4 of 4

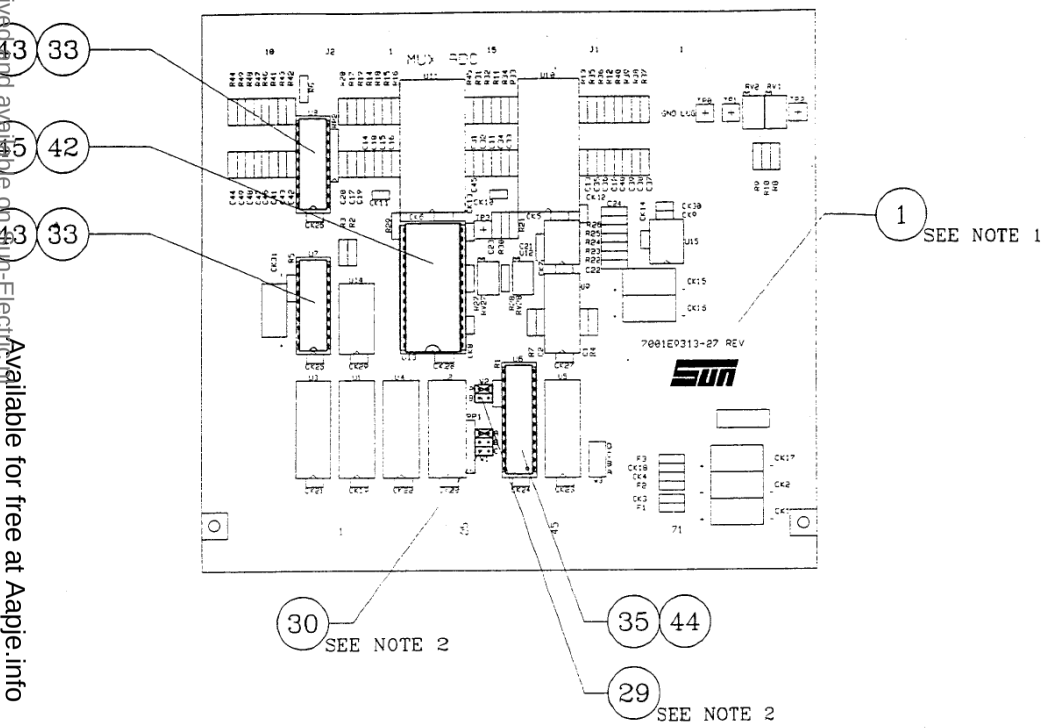
Project no.

Rev B

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Rev	Date	Revisions Description	Check	Appr
A	03'94	ERN 1124 R.F.P.	PT	BG
B	05'95	ECN 5.05.055E CHD QTY ITEM 21 WAS 1 & ITEM 23 WAS 55. MOVED C11,C20,C45 C46 & C49 FROM ITEM 24 TO 21 MOVED ITEM 22 TO 23 ECT. INSERTED NEW LINE AT 22.	O.B	B.G
C	05'95	ECN 5.05.068E P/N CHD FROM 0773E0551-64 TO 0773E0552-64 *(ITEM 35)*	O.B.	B.G.



Item	Qty.	Dwg/Part no	Description	Remarks
34	1	0733E0571-64	TRIGGER GAL (MUX ADC)	U8
33	1	0733E0561-64	CONTROL GAL (MUX ADC)	U7
32	2	7096E3055-12	JUMPER	W1,W2
31	1/12	7096E3055-91	JUMPERSTRIP DOUBLE 3 POS	W1
30	1/18	7096E3055-91	JUMPERSTRIP DOUBLE 2 POS	W2
29	1	0679-0453-00	CAPACITOR 100µF 50V	CK17
28				CK16,CK31
27	5	0679-1256-00	CAPACITOR 10µF 35V	CK1,CK2,CK15
26				C31-C44,C47,C4
25				C12-C19,C22,
24	50	0860-0180-08	CAPACITOR 100nF 50V	CK3-CK14,CK18-CK30
23	1	7096E1080-32	CAPACITOR 10nF 50V	C1
22				C46, C49
21	6	0860-0179-25	CAPACITOR 1nF 100V	C11,C20,C24,C45
20	1	0860-0179-17	CAPACITOR 220pF 100V	C2
19	2	0860-0179-04	CAPACITOR 18pF 100v	C21,C23
18	1	0668-0901-00	RESISTOR ZERO OHM	R22
17	2	0685-0448-06	POTMTR PC MNT (25 TURN)	RV1,RV2
16	2	7096E0085-14	RES. NETWORK 5*10K	RP1,RP2
15	1	1670-3304-00	RES. 33K 0.25W 1%	R30
14	2	1670-2214-00	RES. 22K1 0.25W 1%	R2,R3
13	1	1670-1744-00	RES. 17K4 0.25W 1%	R4
12	1	1670-1074-00	RES. 10K7 0.25W 1%	R9
11	1	1670-6493-00	RES. 6K49 0.25W 1%	R7
10	1	1670-5113-00	RES. 5K11 0.25W 1%	R10
9	1	1670-4993-00	RES. 4K99 0.25W 1%	R25
8	2	1670-4703-00	RES. 4K7 0.25W 1%	R21,R29
7	1	1670-3483-00	RES. 3K48 0.25W 1%	R8
6	1	1670-2213-00	RES. 2K21 0.25W 1%	R24
5	29	1670-2003-00	RES. 2K 0.25W 1%	R11-R20,R31-R49
4	1	1670-1693-00	RES. 1K69 0.25W 1%	R26
3	3	1670-1002-00	RES. 100E 0.25W 1%	R1,R5,R6
2	2	1670-4991-00	RES.49E9 0.2	R27,R28
1	1	7025E9313-27	PCB MUX ADC BOARD	

Item	Qty.	Dwg/Part no	Description
52	REF	0692E9310-25	TEST & CALIBRATION PROCE
51	REF	0692E9310-24	FUNCTIONAL DESCRIPTION M
50	REF	7092E9313-27	SCHEMATIC MUX ADC BOARD
49			
48	1	0681-0802-06	CARD EXTRACTOR
47	4	7096E7075-02	TEST BUTTON TP0,TP1,TP2,TP3
46	3	0739-0106-07	PICO FUSE 1A F1,F2,F3
45	1	7096E3056-07	IC SOCKET 28 PINS U13
44	1	7096E3056-05	IC SOCKET 24 PINS U6
43	2	7096E3056-04	IC SOCKET 20 PINS U7,U8
42	1	7096E2080-64	IC HADC574ZBC U13
41	2	7096E2080-59	IC 74HCT541 U1-U5
40	2	7096E2070-25	IC ADG526 U10,U11
39	1	7096E2070-24	IC AD712JN U12
38	1	7096E2070-22	IC DG419 U15
37	1	0773-8014-00	IC 74HCT4538 U9
36	1	0773-6901-00	IC 74C901 U14
35	1	0773E0552-64	DECODER GAL (MUX ADC) U6

NOTE:
1) ADD CURRENT REVISION LEVEL
2) JUMPER SETTINGS
   W1: A INSTALLED
       B NOT INSTALLED
       C NOT INSTALLED
   W2: A INSTALLED
       B NOT INSTALLED
   W3: A DEFAULT IN COPPER
       B NOT INSTALLED
       C NOT INSTALLED
       D NOT INSTALLED

Scale	N.T.S.	Date	Used in MCS/OCS
Designed by	KEES STAM	03-94	Material
Drawn by	R. V/D HOEF	03-94	
Checked by	PETER TEL	03-94	
Approved	BERNARD GEE	03-94	Finish

Unless otherwise specified : Dimensions are in mm ; Tolerances on : Angles ±5° Holes ±01 Rest ±0.5
Remove all sharp corners and remove burrs

Description: PCB ASSY MUX ADC
Dwg no: 7001E9313-27

SUN ELECTRIC EUROPE B.V. | A2 | Sheet 1 of 1 | Project no | Rev. C

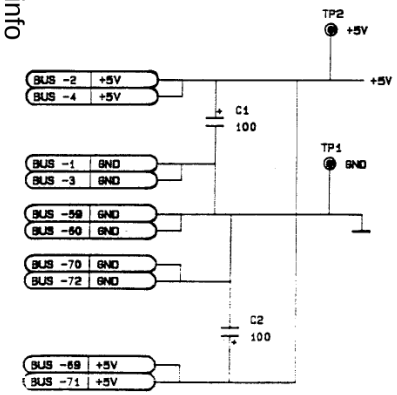
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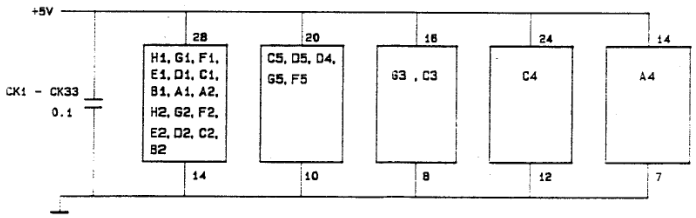
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Revisions					
Rev	Date	ECN	Description	Check	Appr
A	10-88		ERN # 0270. REL. FOR PROD.	GK	JM
B	04-93	3.04.040E	INSERTED IC'S C1, C2, B1, B2 (SHEET 2)	G.K.	BG
C	04-94	4.01.015E	CHG'D PAL TO GAL. DEL'D SHT 3 OF 3 PAL-EPROM LISTING		BG

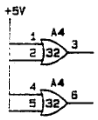
BUS CONNECTOR					
PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	GND	25	BA1	49	/INT6
2	+5V	26	BA9	50	/MEMEN
3	GND	27	BA2	51	/INT5
4	+5V	28	BA10	52	/INT3
5	+12V	29	BA3	53	/INT4
6	-12V	30	BA11	54	/INT2
7	TRSCOPE	31	BA4	55	
8	TRSCOPE	32	BA12	56	/PPRESET
9	BD0	33	BA5	57	/INIT
10	BD8	34	BA13	58	READY
11	BD1	35	BA6	59	GND
12	BD9	36	BA14	60	GND
13	BD2	37	BA7	61	MEMRD
14	BD10	38	BA15	62	IORD
15	BD3	39	BA8	63	MEMWR
16	BD11	40	BA16	64	IOWR
17	BD4	41	BA17	65	/BLDS
18	BD12	42		66	/BUDS
19	BD5	43	BA19	67	
20	BD13	44	BA18	68	
21	BD6	45	BA21	69	+5V
22	BD14	46	BA20	70	GND
23	BD7	47	BR/W	71	+5V
24	BD15	48	CLK4M	72	GND

POWER CONNECTIONS:





SPARES:



NOTES:
1/ UNLESS OTHERWISE SPECIFIED:
  A/ ALL RESISTORS ARE IN OHMS, 1/4W, 5%
  B/ ALL CAPACITORS ARE IN MICRO-FARADS
  C/ ALL DIODES ARE 1N914 OR 1N4148
  D/ ALL IC'S ARE 74LS-SERIES TYPE
  E/ ALL POLARIZED CAPACITORS ARE 16V
2/ LAST USED NO'S: RP4 , C2 , W4 , TP2 , CK33

3/ NOT USED NO'S:

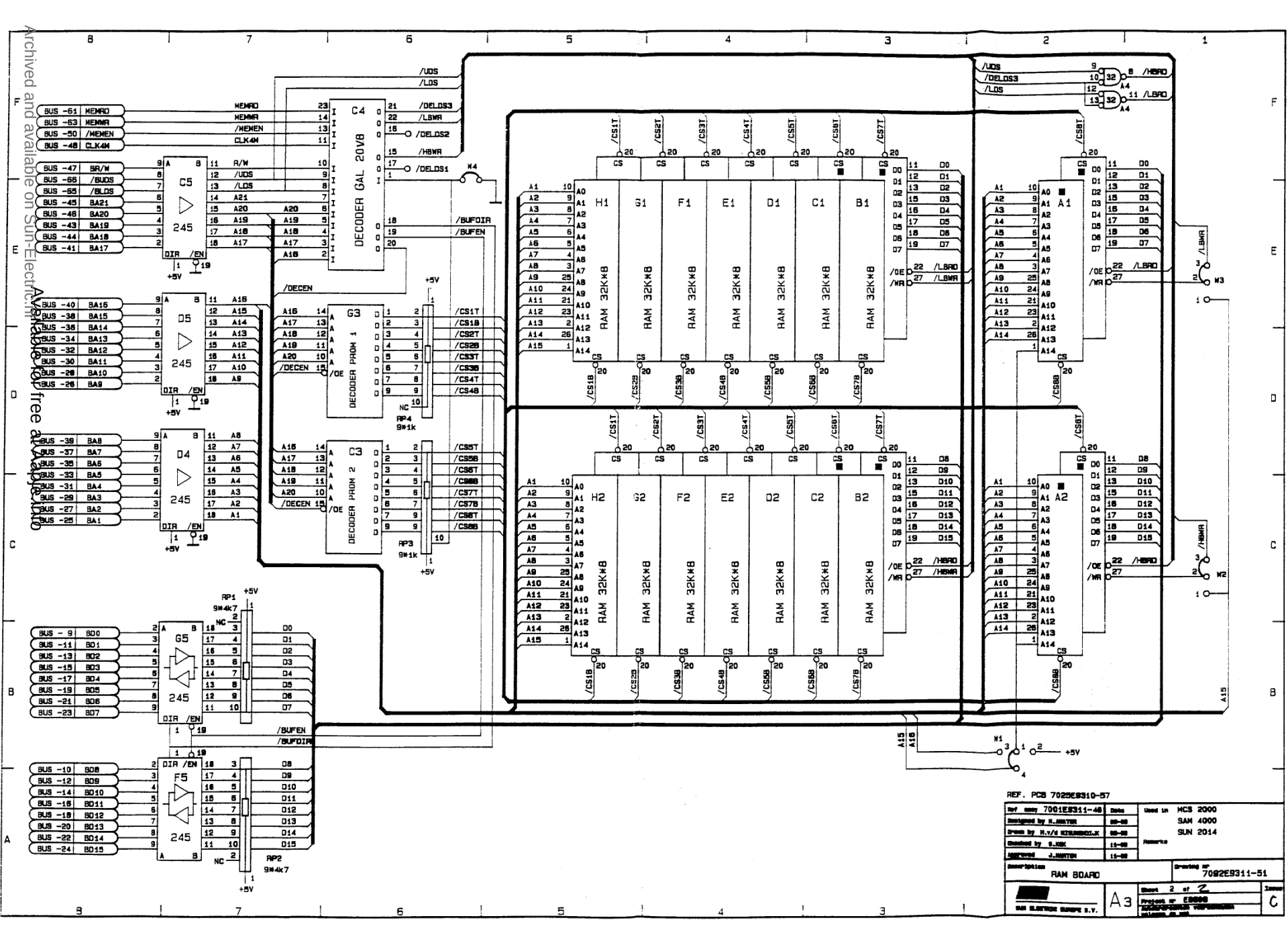
4/ ITEMS MARKED WITH ■ ARE NOT INSERTED.

5/ JUMPERSETTINGS:
  W1: DEFAULT 1-4
  W2: DEFAULT 2-3
  W3: DEFAULT 2-3
  NOTE: W1, W2 AND W3 ARE SET FOR RAM
  W4: IN (FOR USE WITH ECPU68K) DEFAULT
    OUT (FOR USE WITH OLD CPU/RAM REV.D)

REF. PCB 7025E9310-57

Mfr assy 7001E9311-48	Date	Used in	MCS 2000
Designed by M.AMATEN	08-88		SAM 4000
Drawn by H.v/d KERKHOF	08-88		SUN 2014
Checked by G.KOK	11-88	Remarks	
Approved J.MARTEN	11-88		
Description RAM BOARD		Drawing nr 7092E9311-51	
	A3	Sheet 1 of 2	Issue C
		Project nr E8808	

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REF. PCB 7025E9310-57

Ref assy 7001E9311-48	Date	Used in	MCS 2000
Designed by H.MARTEN	88-08		SAM 4000
Drawn by H.v/d HEIJNBOCK	88-08		SUN 2014
Checked by S.KOK	15-09	Remarks	
Approved J.MARTEN	15-09		

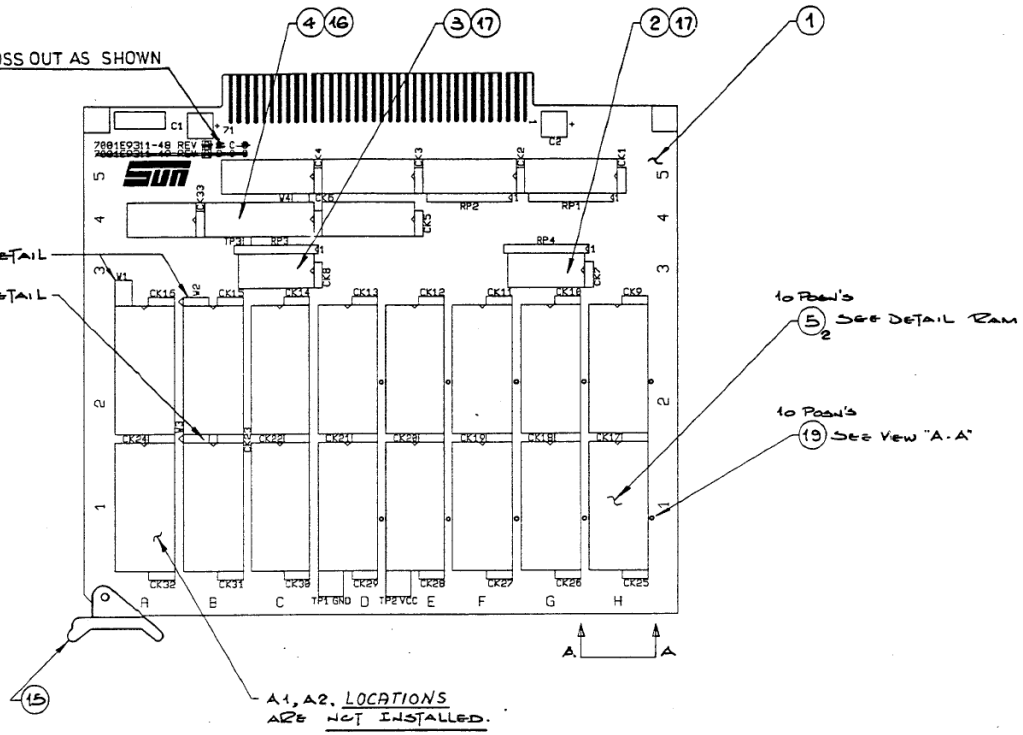
Description: RAM BOARD

Drawing nr 7092E9311-51

SUN ELECTRONICS EUROPE B.V. | A3 | Sheet 2 of 2 | Project nr E9000 | Issue C

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REVISIONS					
SYM	DATE	E-CN	DESCRIPTION	CHECK	APPR.
A	11.10.88	—	ERN #0270	G.K.	J.M
B	04-93	3.04.040E	P/N ITEM 5 WAS 7096E2080-24 QTY ITEM 5 WAS 20	G.K.	BG.
C	04-94	401.015E	CHG'D PR TO GAL	Ø	BG

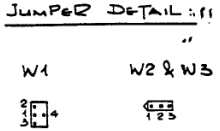


LINE NR	DIRECT ASSEM PART NR	QUAN.	COMPONENTS & SUB ASSEMBLIES		B/M PAGE NR ITEM NR.
1	7025E9310-57	1	PCB RAM/ERAM BOARD		G3 (A2006)
2	0703E0371-01	1	DECODER 1 PROM		C3 (A2007)
3	0703E0381-01	1	DECODER 2 PROM		C4 (A1019)
4	0733E032▪-64	1	DECODER GAL		
5	7096E2080-82	24	RAM TC55257	Top+Bottom	D1, 2...H1, 2
6				Bottom only	B1, B2, C1, C2
7	0773-7245-00	5	IC 74LS245N		C5 D5 D4
8					G5 F5
9	0773-7032-00	1	IC 74LS32		A4
10	7096E1055-13	2	CAPACITOR 100µF/16V TANT.		C1 C2
11	7096E1080-13	32	CAPACITOR 0.1µF CERAMIC		CK1...CK32
12	7096E3055-12	4	JUMPER		W1...W4
13	7096E3055-05	2	JUMP.STRIP 3POS 1 MAKES 12		W2 W3
14	7096E3055-05	1	JUMP.STRIP 2POS 1 MAKES 18		W4
15	0681-0802-06	1	CARD EXTRACTOR		
16	7096E3056-05	1	IC SOCKET 24 PIN		C4
17	7096E3056-02	2	IC SOCKET 16 PIN		C3 G3
18	0536-0302-00	2	TESTPOINT		TP1 TP2
19	7096E3056-46	10	SIP.SOCKET 1POS 1 MAKES 20		
20	7096E0085-07	2	RES.NETW.9▪ 1KO SIL		RP3 RP4
21	0779-0116-00	2	RES.NETW.9▪ 4K7 SIL		RP1 RP2
22	7096E3055-91	1	JUMP.STRIP 3POS 1 MAKES 12		W1
23					
24					
25					
26					
27					
28					
29					
30	7092E9311-51		SCHEMATIC RAM BOARD		REF. ONLY
31	0692E9305-91		FUNCTIONAL DESCRIPTION		REF. ONLY
32					
33					
34					
35					
36					
37					
38					
39					
40					

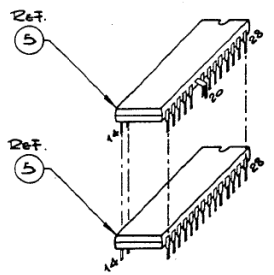
JUMPER SETTINGS:

W1: 1-4
W2: 2-3
W3: 2-3
W4: IN

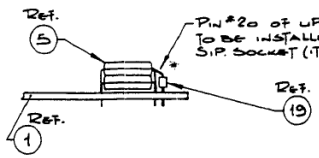
JUMPER DETAIL:



RAM DETAIL SEE NOTE 1



VIEW "A-A"



NOTES:

1) ALL PINS OF BOTH RAM'S (UPPER & LOWER) TO BE SOLDERED PARALLEL, EXCEPT PIN #20 OF UPPER RAM.
BEND PIN #20 OF UPPER RAM AS SHOWN.

Scale 1:1	Date	Used in MCS 2000, SUN 2014 & SAM 4000	
Designed by		Material	
Drawn by TJIN A SOE M.	11.11.88		
Checked by G. KOK.	15.11.88		
Approved J. M. Lenten	17-11-88	Finish	
Unless otherwise specified: Dimensions are in mm; Tolerances on: Angles ± 0.5 Holes ± 0.1 Rest ± 0.5			
Remove all sharp corners and remove burrs			
Description PCB Ass'y RAM		Dwg. no 7001E9311-48	
SUN ELECTRONICS B.V.	A2	Sheet 1 of 1	Issue C
		Code	
		Project no. E3808	

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Available for free at Aapje.info

Revisions				
Rev	Date	ECN	Description	Check / Appr
A	10-88		ERN # 0270.REL. FOR PROD.	G.K.
B	04-89	4.01. 017E	CHANGED PAL'S TO GAL'S DELD SHEET 6 OF 6, PAL-LISTINGS	

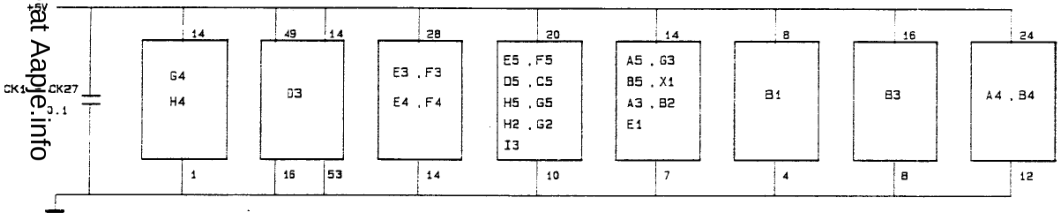
BUS CONNECTOR

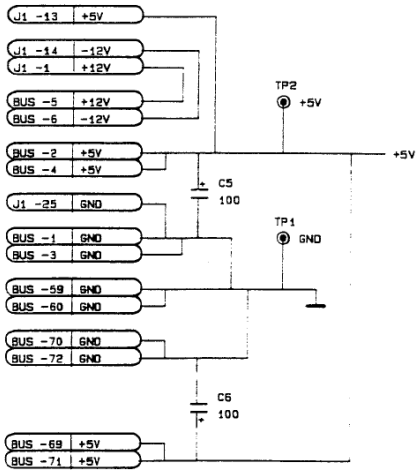
PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	GND	25	BA1	49	/INT6
2	+5V	26	BA9	50	/MEMEN
3	GND	27	BA2	51	/INT5
4	+5V	28	BA10	52	/INT3
5	+12V	29	BA3	53	/INT4
6	-12V	30	BA11	54	/INT2
7	TRSCOPE	31	BA4	55	
8	TRSCOPE	32	BA12	56	/PPRESET
9	BD0	33	BA5	57	/INIT
10	BD8	34	BA13	58	READY
11	BD1	35	BA6	59	GND
12	BD9	36	BA14	60	GND
13	BD2	37	BA7	61	MEMRD
14	BD10	38	BA15	62	IORD
15	BD3	39	BA8	63	MEMWR
16	BD11	40	BA16	64	IOWR
17	BD4	41	BA17	65	/BLDS
18	BD12	42		66	/BUDS
19	BD5	43	BA19	67	
20	BD13	44	BA18	68	
21	BD6	45	BA21	69	+5V
22	BD14	46	BA20	70	GND
23	BD7	47	BR/W	71	+5V
24	BD15	48	CLK4M	72	GND

J1 25P D FEMALE

PIN NO.	SIGNAL
1	+12V
2	D3
3	D4
4	D5
5	D6
6	D7
7	VMA
8	E
9	/IRQ7
10	/INIT
11	R/W
12	/IACK7
13	+5V
14	-12V
15	D2
16	D1
17	D0
18	/IRQACIA
19	/CSACIA
20	A4
21	A3
22	A2
23	A1
24	A5
25	GND

POWER CONNECTIONS:





NOTES:

1/ UNLESS OTHERWISE SPECIFIED:
- A/ ALL RESISTORS ARE IN OHMS, 1/4W, 5%
- B/ ALL CAPACITORS ARE IN MICRO-FARADS
- C/ ALL DIODES ARE 1N914 OR 1N4148
- D/ ALL IC'S ARE 74LS-SERIES TYPE
- E/ ALL POLARIZED CAPACITORS ARE 16V

2/ LAST USED NO'S: R5, RP9, C6, W8, J1, S1, X1, TP2, LED6

3/ NOT USED NO'S:

4/ JUMPERSETTINGS :

W1 : DEFAULT NOT INSTALLED
INSTALL IF SGA 9000 IS CONNECTED

W2 : DEFAULT IN COPPER
DEBUG IRQ7

W3 : DEFAULT NOT INSTALLED

W4 : DEFAULT 1-2

W5 : DEFAULT 1-2

W6 : DEFAULT 1-2

NOTE : W5 AND W6 ARE SET FOR 27256 EPROM

W7 : DEFAULT NOT INSTALLED

W8 : DEFAULT INSTALLED

REF. PCB 7025E9310-56

Ref spec 7001E9311-44	Date	Used in	MCS 2000
Designed by H.AMATER	07-88		SAM 4000
Drawn by H.v/d HIELKEMOLK	07-88		SUN 2014
Checked by G.KOK	11-88	Remarks	POWER DISTRIBUTION
Approved V. Marten	11-88		

Description: ECPU68K BOARD
Drawing nr: 7092E9311-47
SUN ELECTRIC EUROPE B.V.
A3
Sheet 1 of 5
Project nr E8808
Automatisering verzekeringen adviezen en meer
Issue B

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SIGNAL WHERE USED LIST

NAME	GENERATED (SHT-GRID)	USED (SHT-GRID)
A1	3-5F	3-4F, 2F; 4-6F/E, 6D, 4F, 4D (2*), 2E, 2D; 5-2C, 1C;
A2	3-5F	3-4F, 2F; 4-6E, 6D/C, 4E, 4D (2*), 2E, 2D/C; 5-2C, 1C;
A3	3-5F	3-4F, 2F; 4-6E, 6C, 4E, 4D (2*), 2E, 2C; 5-2C/B, 1C/B;
A4	3-5F	3-4F, 2F; 4-4E, 4C, 2E, 2C; 5-2B, 1B;
A5	3-5E	3-4E, 2F; 4-4E, 4C, 2E, 2C; 5-2B, 1B;
A6	3-5E	3-4E, 2F/E; 4-4E, 4C, 2E, 2C;
A7	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A8	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A9	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A10	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A11	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A12	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A13	3-5E	3-4E, 2E; 4-4E, 4C, 2E, 2C;
A14	3-5E	3-4E, 2E/D; 4-4E/D, 4C, 2E/D, 2C;
A15	3-5E	3-4E, 2D; 4-5E, 2D, 2C/B;
A16	3-5D	3-4D, 2D; 4-5B;
A17	3-5D	3-4D, 2D;
A18	3-5D	3-4D, 2D;
A19	3-5D	3-4D, 2D;
A20	3-5D	3-4D, 2D;
A21	3-5D	3-4D, 2D, 4E;
A22	3-5D	3-4D, 4E;
A23	3-5D	3-4D, 4E;
AS	3-4D	3-4D, 4E, 3D;
/AAS	3-5D	3-2D/C, 5D;
BA1	3-1F	3-1F;
BA2	3-1F	3-1F;
BA3	3-1F	3-1F;
BA4	3-1F	3-1F;
BA5	3-1F	3-1F;
BA6	3-1F/E	3-1F/E;
BA7	3-1E	3-1E;
BA8	3-1E	3-1E;
BA9	3-1E	3-1E;
BA10	3-1E	3-1E;
BA11	3-1E	3-1E;
BA12	3-1E	3-1E;
BA13	3-1E	3-1E;
BA14	3-1E/D	3-1E/D;
BA15	3-1D	3-1D;
BA16	3-1D	3-1D;
BA17	3-1D	3-1D;
BA18	3-1D	3-1D;
BA19	3-1D	3-1D;
BA20	3-1D	3-1D;
BA21	3-1D	3-1D;
BD0	3-8F	3-8F;
BD1	3-8F	3-8F;
BD2	3-8F	3-8F;
BD3	3-8F/E	3-8F/E;
BD4	3-8E	3-8E;
BD5	3-8E	3-8E;
BD6	3-8E	3-8E;
BD7	3-8E	3-8E;
BD8	3-8E	3-8E;
BD9	3-8E	3-8E;
BD10	3-8E	3-8E;
BD11	3-8E	3-8E;
BD12	3-8E/D	3-8E/D;
BD13	3-8D	3-8D;
BD14	3-8D	3-8D;
BD15	3-8D	3-9D;
/BLDS	3-1C	3-1C;
/BRESET	3-4A	3-4/3B; 4-6B, 6D; 5-5E, 5D;
BR/W	3-1C	3-1C;
/BUDS	3-1C	3-1C;
/CLK	3-7D	3-6D, 2C;
CLK4M	3-1C	3-1C;
/CSACIA	3-3F	5-2E, 1C;
/CSBOOT	3-3D	4-3B, 3D;
/CSE2	3-3D	4-2C, 2E/D;

SIGNAL WHERE USED LIST

NAME	GENERATED (SHT-GRID)	USED (SHT-GRID)
/CSTIM1	3-3F/E	4-6E;
/CSTIM2	3-3E	4-6C;
/CSREG	3-3E	5-5C, 5E;
D0	3-6F 5-1F/E	4-6C, 3E, 2E; 5-2F/E, 1F/E;
D1	3-6F 5-1E	4-6C, 3E, 2E; 5-2E, 1E;
D2	3-6F 5-1E	4-6C, 3E, 2E; 5-2E, 1E;
D3	3-6F/E 5-1E	4-6C, 3E, 2E; 5-5E, 2E, 1E;
D4	3-6E 5-1E	4-6C, 3E, 2E; 5-5E, 2C, 1C;
D5	3-6E 5-1E	4-6C, 3E, 2E; 5-5E, 2E, 1E;
D6	3-6E 5-1E	4-6C, 3E, 2E; 5-5E, 2E, 1E;
D7	3-6E 5-1E	4-6C, 3E, 2E; 5-5E, 2E, 1E;
D8	3-6E	4-3C, 1D;
D9	3-6E	4-3C, 1C;
D10	3-6E	4-3C, 1C;
D11	3-6E	4-3C, 1C;
D12	3-6E/D	4-3C, 1C;
D13	3-6D	4-3C, 1C;
D14	3-6D	4-3C, 1C;
D15	3-6D	4-3C, 1C;
/DTACK	3-3E	3-4C;
E	3-6B	4-6E, 6C; 5-3C, 1C;
/E2BUSY	4-1D	5-7D;
/HBRD	4-6B/A	4-3C;
/HBWR	4-6A	4-2B;
/IACK	3-4C	3-4E;
/IACK3	3-3E	5-6D;
/IACK7	3-3E	5-1C;
/INIT	3-3C/B	3-1B (2*)
/INT2	4-8C	4-7C;
/INT3	4-8C	4-7C;
INT4	3-1C/B	4-8D;
/INT4	3-1B	3-2B/C;
INT5	3-1B	4-8E;
/INT5	3-1B	3-2B;
/INT6	4-8E	4-7E;
IORD	3-1C	3-1C;
/IORD	3-3D	3-2C;
IOWR	3-1C	3-1C;
/IOWR	3-3D	3-2C;
/IRQACIA	3-8C	3-8C, 7C;
/IRQ1	4-6D	3-7A;
/IRQ2	4-6B	3-7A, 7C, 7B;
/IRQ3	5-6D	3-7A, 7C, 7B;
/IRQ7	3-8C	3-8C, 7C;
/LBRD	4-4B/A	4-1E, 3E;
/LBWR	4-4B/A	4-1D;
/LDS	3-5D	3-4D, 2C, 4E; 4-5A (2*);
/MEMEN	3-1D/C	3-1D/C;
/MEMRD	3-1C	3-1C;
/MEMWR	3-1C	3-1C;
/ONBOARD	3-3D	3-3E/D;
/PPRESET	5-4D/C	5-1D/C;
READY	3-1B	3-5C;
R/W	3-5C	3-4/3B; 4-6A, 5A/B, 6B, 6D; 5-2C, 1C;
STARTUP	3-3B	3-3C;
/UDS	3-5D	3-4D, 2C, 4E; 4-6A (2*);
VMA	3-6B	4-6C/B, 6E/D; 5-2C, 1C;
/VPA	3-4C	3-5C (2*);
W/R	3-5C	3-4C, 2C; 4-6B, 5B;

REF. PCB 7025E9310-56

Ref assy 7001E9311-44	Date	Used in	MCS 2000
Designed by M.AMATER	09-88		SAM 4000
Drawn by H.v/d WIELENDDIJK	09-88		SUN 2014
Checked by G.VOK.	11-88	Remarks	
Approved J. v/d Linden	11-88		SIGNAL WHERE USED LIST

Description: ECPU68K BOARD

Drawing nr: 7092E9311-47

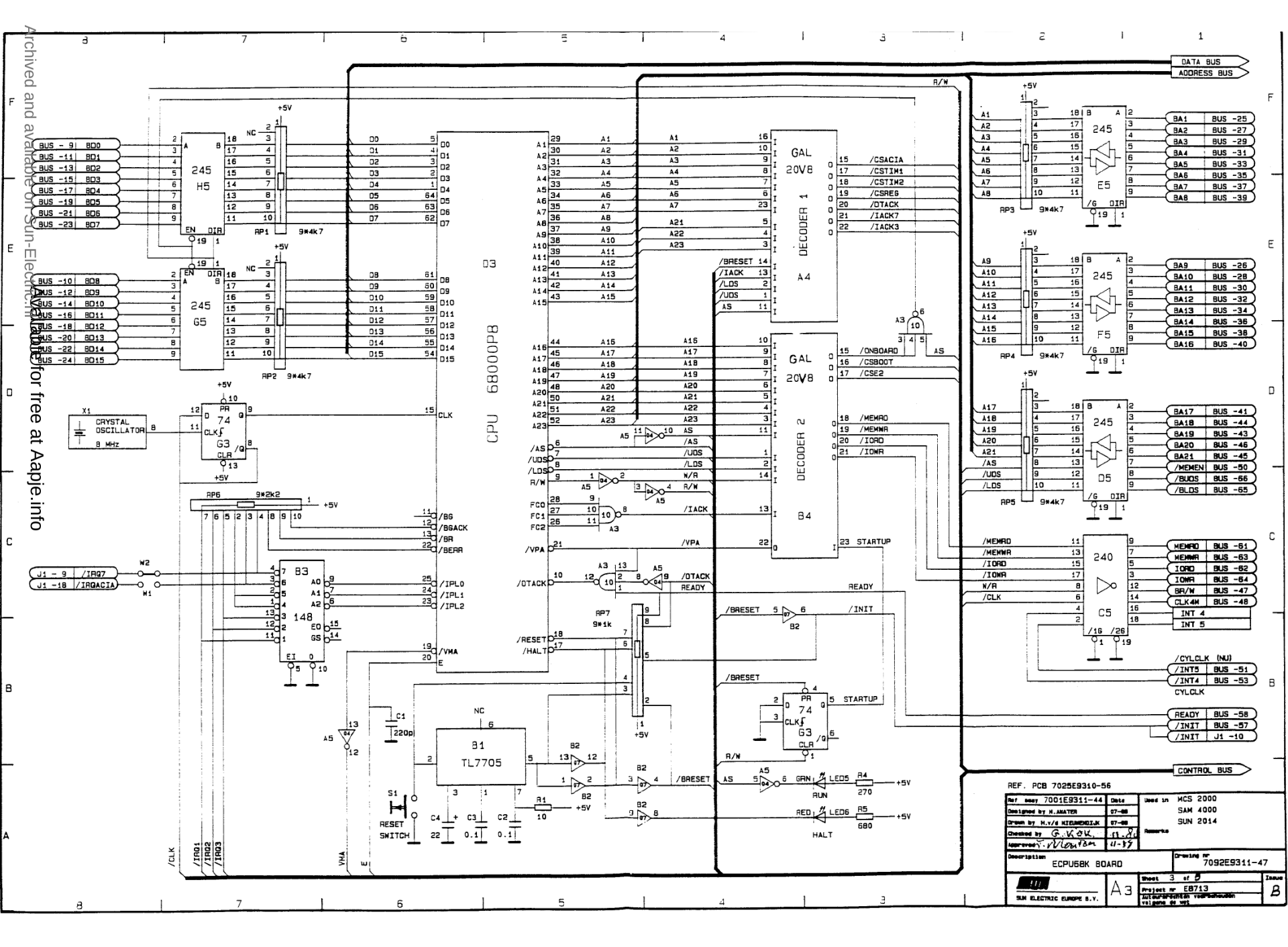
SUN ELECTRIC EUROPE B.V.

A3

Sheet 2 of 5

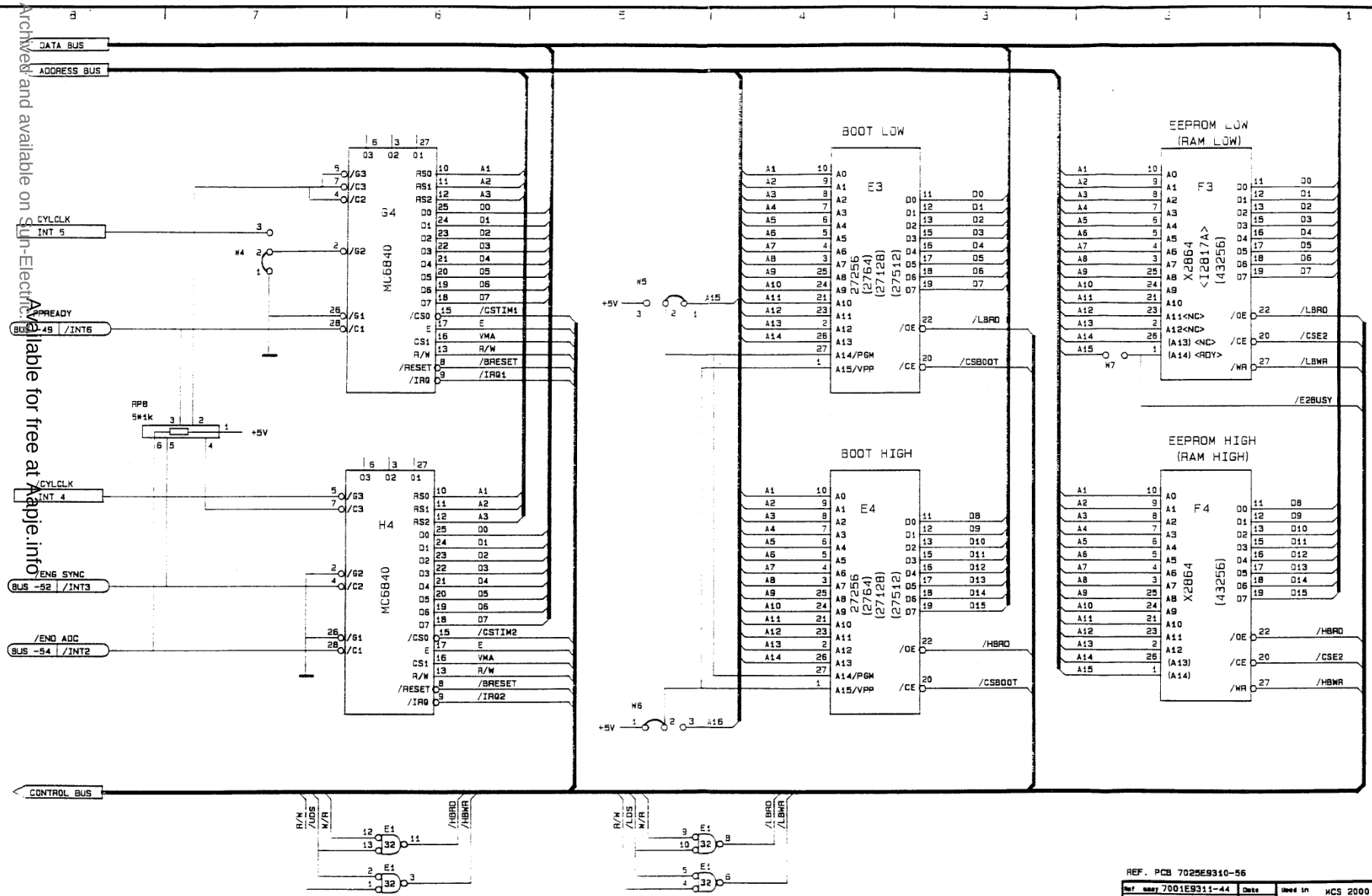
Project nr E8808

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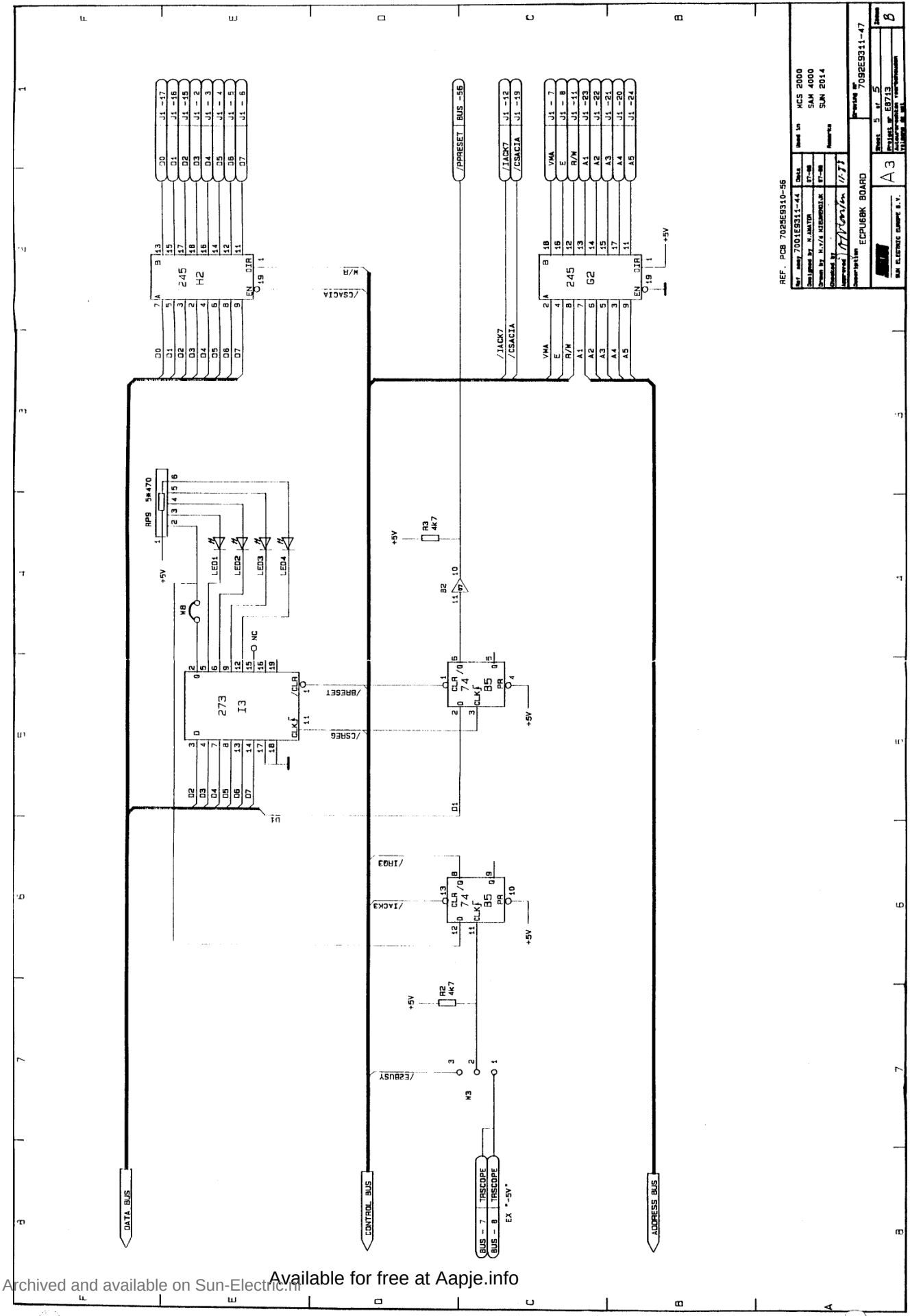
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REF. PCB 7025E9310-56

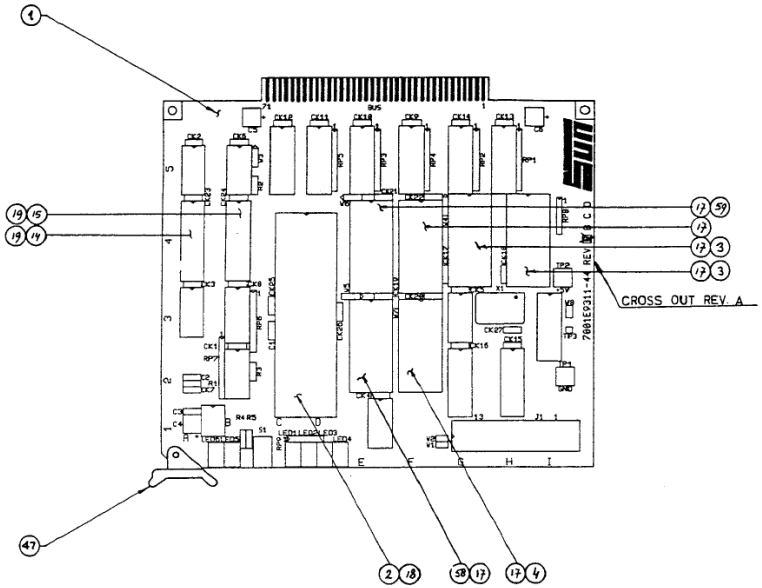
Ref assy 7001E9311-44	Date	Used in	MCS 2000
Designed by N.AMATOR	87-08		SAM 4000
Drawn by H.v/d KIEUMENDIJK	87-08		SUN 2014
Checked by J. Martin	11-87	Remarks	
Approved J. Martin	11-87		
Description ECPU68K BOARD		Drawing nr 7092E9311-47	
SUN ELECTRIC EUROPE B.V.	A3	Sheet 4 of 5	Issue B
		Project nr E8713	
		Auteursrechten voorbehouden raadpleeg de wet	



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Rev	Date	ECN	Revisions Description	Check	Appr
A	14.6.88	—	6824 e 0870	G.K.	JAM
B	04-94	401-0176	CHG'D PHOTO GRLS		Bg



LINE NR	DIRECT ASSEM PART NR.	QUANT	COMPONENTS & SUB ASSEMBLIES	ITEM NR.
1	7025E9310-56	1	PCB ECPU 68K	
2	003-0776-665	1	IC MC68000P8	D3
3	0773-0277-00	2	IC MC6840T100	G4, H4
4	0773-0457-00	1	IC D2817A-1	F3
5	0773-7004-00	1	IC 74LS04	A5
6	0773-7007-00	1	IC 7407	B3
7	0773-7010-00	1	IC 74LS10	A3
8	0773-7032-00	1	IC 74LS32	E1
9	0773-7074-00	2	IC 74LS74	B5, G3
10	0773-7148-00	1	IC 74LS148	B3
11	0773-7240-00	1	IC 74LS240	C5
12	0773-7245-00	7	IC 74LS245	E5, F5, D5, G2 H5, G5, H2
13				
14	0733E039*-64	1	DECODER 1 GAL	A4
15	0733E031*-64	1	DECODER 2 GAL	B4
16	7096E1080-33	1	IC TL7705	B1
17	7096E1056-07	6	IC SOCKET 28 PIN	
18	7096E1056-11	1	IC SOCKET 64 PIN	
19	7096E1056-05	2	IC SOCKET 24 PIN	
20	7096E7075-02	2	TEST POINT	TP1, TP2
21	7096E1080-13	29	CAPACITOR 0.1µF CERAMIC	CK1"CK27, C2, C3
22				
23	7096E1055-13	2	CAPACITOR 10µµF 16V TANTALUM	C5, C6
24	0860-0173-16	1	CAPACITOR 220pF CERAMIC	C1
25	7096E1055-11	1	CAPACITOR 22µF 16V TANTALUM	C4
26	0680-2001-00	1	RESISTOR 10R 5% WM	R1
27	0680-2067-00	2	RESISTOR 4K7 5% WM	R2, R3
28	0680-2030-00	1	RESISTOR 270R 5% WM	R4
29	0680-2061-00	1	RESISTOR 680R 5% WM	R5
30	7096E0085-09	1	RESISTOR NETWORK 9 * 2K2 SIL	RP6
31	0779-0116-00	5	RESISTOR NETWORK 9 * 4K7 SIL	RP1"RP5
32	7096E0085-07	1	RESISTOR NETWORK 9 * 1K0 SIL	RP7
33	7096E0085-11	1	RESISTOR NETWORK 5 * 1K0 SIL	RP8
34	0779-0150-00	1	RESISTOR NETWORK 5 * 470E SIL	RP9
35	003-0689-562	1	PUSH BOTTON SWITCH	S1
36	7096E1055-12	4	JUMPER	W4, W5, W6, W8
37	7096E1055-05	3	JUMPER STRIP 2 POS (1 MAKES 18)	W1, W3, W7
38	7096E1055-05	4	JUMPER STRIP 3 POS (1 MAKES 12)	W2"W6
39	003-3931-525	1	CONNECTOR 25 PIN 90°	J1
40	400-2500-203	2	MASHER EXT. S/P 2.5mm	J1
41	404-2510-523	2	SCREW M2.5 * 10	J1
42	409-2500-103	2	NUT M2.5	J1
43	7096E2055-13	1	LED GRN HLMP 5050 RA	LED 5
44	7096E2055-12	1	LED RED HLMP 5030 RA	LED 6
45	7096E2055-14	4	LED YEL HLMP 5040 RA	LED 1...4
46	7096E2080-42	1	X-TAL OSCILL. 8MHz DIP 14	X1
47	0681-0802-06	1	CARD EXTRACTOR	
48	0773-7273-00	1	IC 74LS273	I3
49				
50				
51				
52				
53				
54				
55	7092E9311-47		SCHEMATIC ECPU 68K	REF. ONLY
56	0692E9305-90		FUNCTIONAL DESCRIPTION	REF. ONLY
57				
58	0703E028*-01		EPROM FIRMWARE (E3)	REF. ONLY
59	0703E028*-02		EPROM FIRMWARE (E4)	REF. ONLY
60				
61				
62			* = 3 or up	
63				
64				
65				
66				
67				
68				
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79				
80				

Notes:

1. Jumper Settings

W1: Default not installed
Install if SGA 5000 is connected.

W2: Default in copper
Debug 1207

W3: Default not installed

W4: Default 1-2

W5: Default 1-2

W6: Default 1-2
Remark: W5 & W6 are set for 27256 EPROM.

W7: Default not installed

W8: Default installed

Jumper Detail:

W5, W4, W5 & W6

Item	Qty	Dwg / Part no	Description	Remarks
Scale 4 : 4			Date	Used in MC6 5000, Sun3 E010 & 3000 4000
Designed by				Material
Drawn by Toine A. Sage M.			14.11.88	
Checked by G. KOK.			15.11.88	
Approved J.A. Marten			17-11-88	Finish

Unless otherwise specified: Dimensions are in mm Tolerances on Angles ± 0.5 Holes ± 0.1 Rest ± 0.5

Remove all sharp corners and remove burrs

Description: Pcb Ass'y ECPU 68K

Dwg no: 7096E9311-44

Sun

A1

Sheet 4 of 4

Code

Project no 6824-0870

Issue B.

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Revisions				
Rev	Date	ECN	Description	Check / Appr
A	180987	—	SAN# 0099	S.T. BG
B	04'94	4.01.013E	CHG'D PAL TO GAL DEL'D NOTE 4, "U5" I/O CONFIGURATION	BG BG

J1 CONNECTOR

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	GROUND	37	AB 7
2	+5V	38	
3	GROUND	39	AB 8
4	+5V	40	
5	+12V	41	
6		42	
7		43	
8		44	
9	DB 0	45	
10	DB 8	46	
11	DB 1	47	
12	DB 9	48	
13	DB 2	49	
14	DB 10	50	
15	DB 3	51	
16	DB 11	52	
17	DB 4	53	
18	DB 12	54	
19	DB 5	55	
20	DB 13	56	
21	DB 6	57	/INITIALB
22	DB 14	58	
23	DB 7	59	
24	DB 15	60	
25	AB 1	61	
26	AB 9	62	IO RDB
27	AB 2	63	
28	AB 10	64	IO WRB
29	AB 3	65	/LDSB
30	AB 11	66	
31	AB 4	67	
32	AB 12	68	+12V
33	AB 5	69	+5V
34		70	GROUND
35	AB 6	71	+5V
36		72	GROUND

P2 CONNECTOR

PIN NO.	SIGNAL
1	/STB
2	GROUND
3	DATA 0
4	GROUND
5	DATA 1
6	GROUND
7	DATA 2
8	GROUND
9	DATA 3
10	GROUND
11	DATA 4
12	GROUND
13	DATA 5
14	GROUND
15	DATA 6
16	GROUND
17	DATA 7
18	GROUND
19	/ACK
20	GROUND
21	BUSY
22	GROUND
23	PE
24	GROUND
25	SELECT
26	/PRIME
27	/AUTOFEED
28	/ERROR
29	
30	SIGNAL GROUND
31	SIGNAL GROUND
32	
33	FRAME GROUND
34	

P3 CONNECTOR

PIN NO.	SIGNAL
1	/STL STB
2	GROUND
3	STL DATA 0
4	GROUND
5	STL DATA 1
6	GROUND
7	STL DATA 2
8	GROUND
9	STL DATA 3
10	GROUND
11	STL DATA 4
12	GROUND
13	STL DATA 5
14	GROUND
15	STL DATA 6
16	GROUND
17	STL DATA 7
18	GROUND
19	/STL ACK
20	GROUND
21	STL BUSY
22	GROUND
23	STL PE
24	GROUND
25	STLP SELECT
26	/STL PRIME
27	/STL AUTOFEED
28	/STL ERROR
29	
30	SIGNAL GROUND
31	SIGNAL GROUND
32	
33	
34	

P4 CONNECTOR

PIN NO.	SIGNAL
1	VIDEO IN
2	HS IN
3	VS IN
4	GROUND

P5 CONNECTOR

PIN NO.	SIGNAL
1	VIDEO STL
2	STL HS
3	STL VS
4	/STL SELECT
5	/STL SENSE
6	GROUND STL

P6 CONNECTOR

PIN NO.	SIGNAL
1	VIDEO OUT
2	HS OUT
3	VS OUT
4	GROUND

JUMPER TABLE:

			MCS 2000			
OPTION PRESENT	W2	W1	W3		W4	W5
	OUT	OUT	2-4	5-6	OUT	OUT
PRINTER	OUT	IN	2-4	5-6	OUT	OUT
STL 2	IN	OUT	3-4	5-6	OUT	OUT
PRINTER/STL 2	IN	IN	3-4	5-6	OUT	OUT

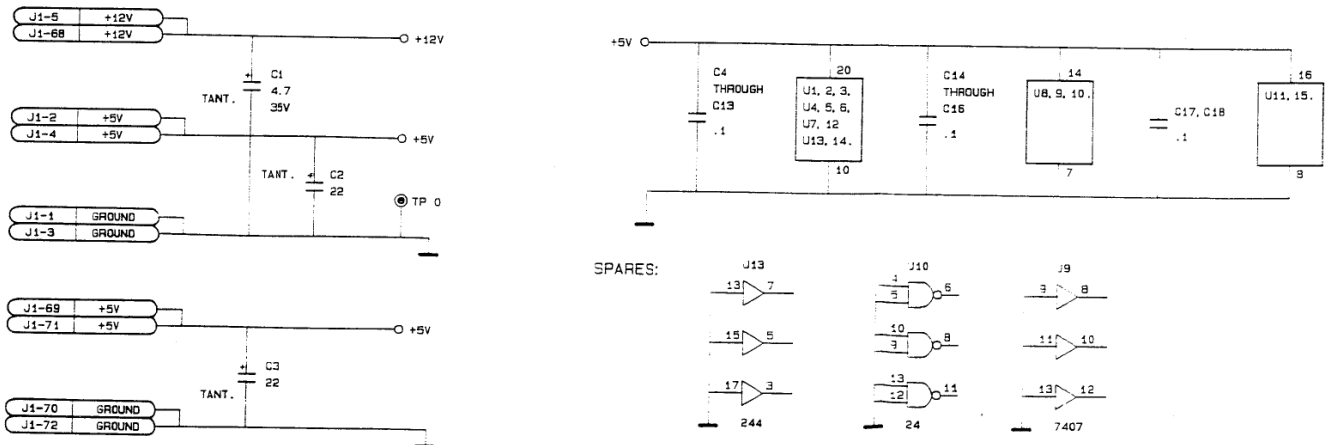
NOTES:

1/ UNLESS OTHERWISE SPECIFIED:
- A/ ALL RESISTORS ARE IN OHMS, 1/4W, 5%
- B/ ALL CAPACITORS ARE IN MICRO-FARADS
- C/ ALL DIODES ARE 1N914 OR 1N4148
- D/ ALL IC'S ARE 74LS-SERIES TYPE
- E/ ALL POLARIZED CAPACITORS ARE 16V

2/ LAST USED NO'S: R5, C20, D2, U15, RP4, LED1, K1, W5, TP0.

3/ NOT USED NO'S:

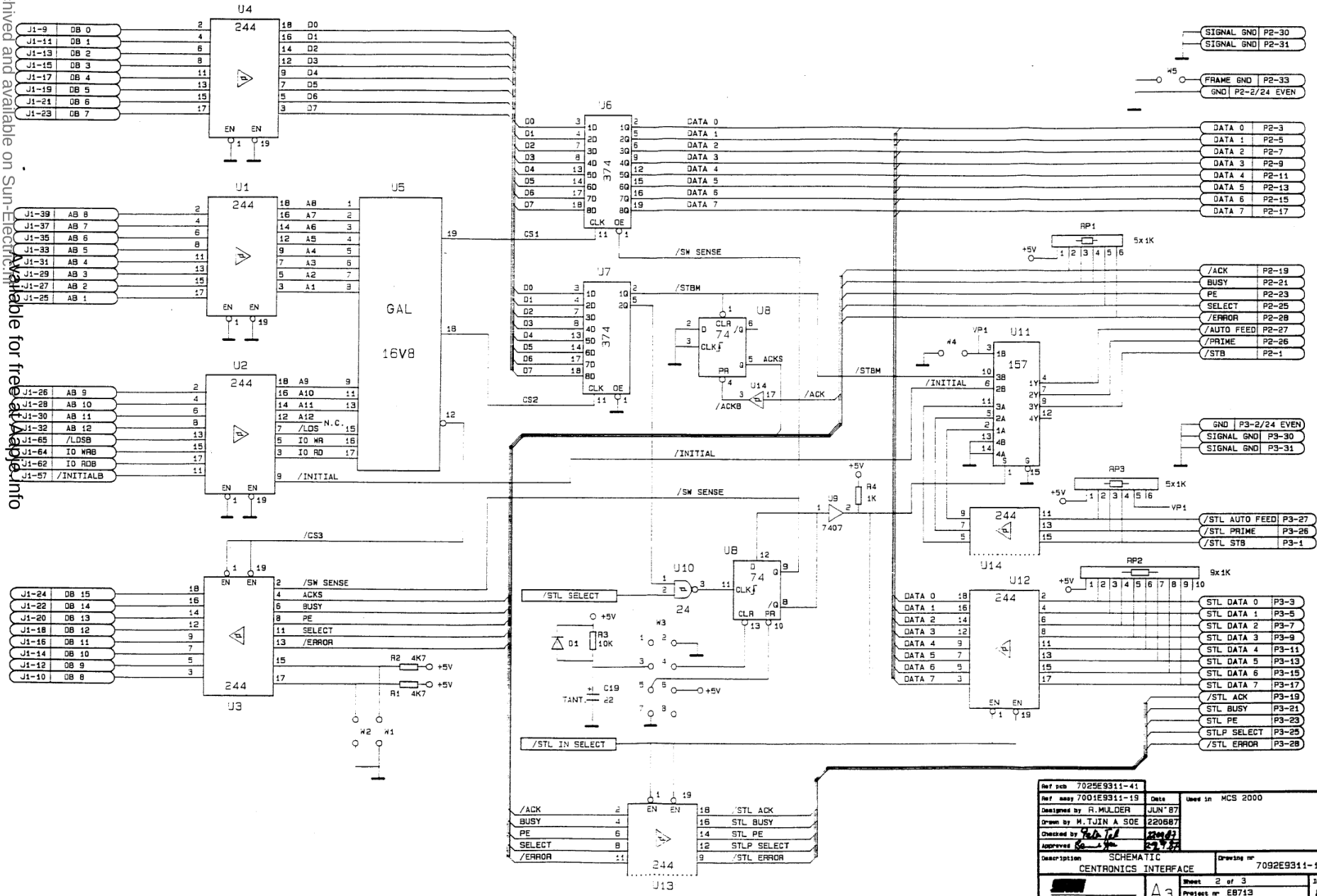
POWER CONNECTIONS:



SPARES:

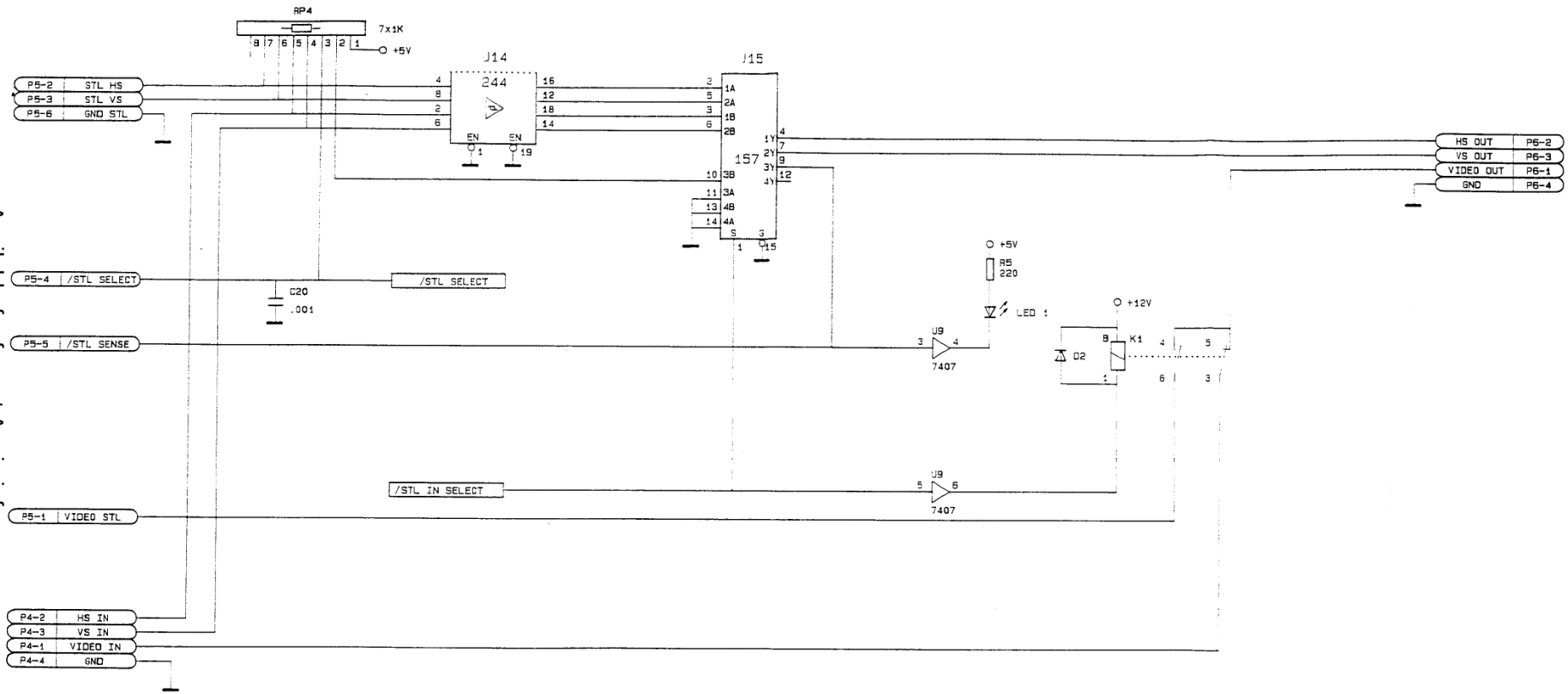
Ref pcb 7025E9310-41			
Ref assy 7001E9311-19	Date	Used in MCS 2000	
Designed by R.MULDER	JUN'87		
Drawn by M.TJIN A SOE	290687		
Checked by Pete Tel	29-6-87		
Approved Bernard Ter	22.3.88		
Description SCHEMATIC CENTRONICS INTERFACE		Drawing nr 7092E9311-18	
SUN ELECTRIC EUROPE B.V.	A3	Sheet 1 of 3	Issue B
		Project nr E8713	

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Ref pcb	7025E9311-41		
Ref assy	7001E9311-19	Date	Used in MCS 2000
Designed by	R.MULDER	JUN'87	
Drawn by	M.TJIN A SOE	220687	
Checked by			
Approved			
Description	SCHEMATIC CENTRONICS INTERFACE		Drawing nr 7092E9311-18
SUN ELECTRIC EUROPE B.V.	A3	Sheet 2 of 3	Issue B
		Project nr E8713	

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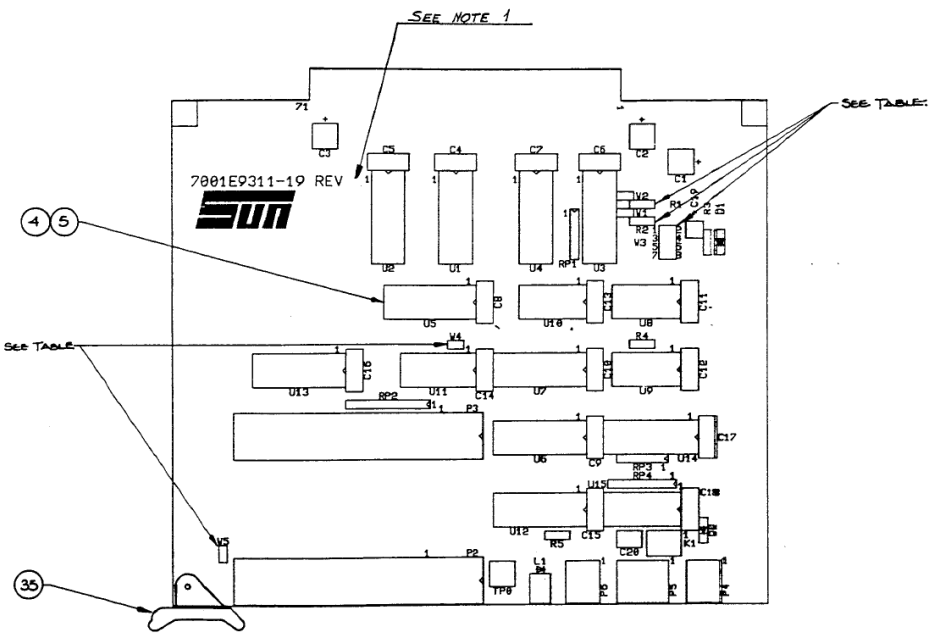


Ref pcb 7025E9310-41			
Ref assy 7001E9311-19	Date	Used in MCS 2000	
Designed by R.MULDER	JUN'87		
Drawn by M.TJIN A SOE	290687		
Checked by			
Approved			
Description SCHEMATIC CENTRONICS INTERFACE		Drawing nr 7092E9311-18	
SUN ELECTRIC EUROPE B.V.	A3	Sheet 3 of 3	Issue B
		Project nr E8713	

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Hole Schedule		
Code	Qty.	Dia.

Revisions					
Sym	Date	ECN	Description	Check	Appr.
A	18.08.87		E-ECN # 0099	P.T.	BB
B	04'94	4.01. 0138	CHANGED PAL TO GAL. ADDED NOTE 1.		BB



NOTES:

1) STAMP CURRENT REV. LEVEL

			MCS 2000		
OPTION PRESENT	W2	W1	W3	W4	W5
——	OUT	OUT	2-4	5-6	OUT	OUT
PRINTER	OUT	IN	2-4	5-6	OUT	OUT
STL2	IN	OUT	3-4	5-6	OUT	OUT
PRINTER/STL2	IN	IN	3-4	5-6	OUT	OUT

LINE NR	DIRECT ASSEM PART NR.	QUANT	COMPONENTS & SUB ASSEMBLIES	ITEM NR.
1	7025E9310-41	1	PCB CENTRONICS INTERFACE	
2	7092E9311-18	REF.	SCHEMATIC CENTRONICS INTERFACE	
3	0773-7244-00	7	IC 74LS244	U1-U4, U12-U14
4	0733E053*-64	1	GAL DECODER	U5
5	003-0776-675	1	IC SOCKET 20 PINS	USED WITH ITEM 4
6	0773-7374-00	2	IC 74LS374	U6, U7
7	0773-7074-00	1	IC 74LS74	U8
8	0773-0236-00	1	IC 7407	U9
9	0773-7024-00	1	IC 74LS24	U10
10	0773-7157-00	2	IC 74LS157	U11, U15
11	003-0680-600	2	RESISTOR 4K7 ¼W 5%	R1, R22
12	0680-2075-00	1	RESISTOR 10K ¼W 5%	R3
13	003-0680-642	1	RESISTOR 1K ¼W 5%	R4
14	003-0680-606	1	RESISTOR 100R ¼W 5%	R5
15	0679-0411-00	1	CAPACITOR 4µ7 35V TANT.	C1
16	7096E1055-11	3	CAPACITOR 22µ 16V TANT.	C2, C3, C19
17	0679-1325-00	25	CAPACITOR 100n 100V MKMO 0.4"	C4 THRU C18
18	0860-0168-00	1	CAPACITOR 1n CER. DISK	C20
19				
20	0771-0272-00	2	DIODE 1N914 OR 1N4148	D1, D2
21	7096E0085-11	2	RESISTOR PACKAGE 5*1K	RP1, RP3
22	7096E0085-07	1	RESISTOR PACKAGE 9*1K	RP2
23	0779-0144-00	1	RESISTOR PACKAGE 7*1K	RP4
24	7096E2055-12	1	LED RED ANGLED	LED 1
25	7096E4055-33	1	RELAY 22D12-P	K1
26	7096E3055-05	4*2/36	JUMPER STRIP SINGLE ROW	W1, W2, W4, W5
27	7096E3055-91	1*4/36	JUMPER STRIP DOUBLE ROW	W3
28	7096E3055-12	2	JUMPER	W3
29	7096E3055-12	A/R	2 JUMPERS FOR PRINTER & STL-2	W1 & W2
30	7096E3055-12	A/R	1 JUMPER FOR PRINTER OR STL-2	W1 OR W2
31	003-0606-524	1	TEST POINT	TP0
32	003-3931-949	2	CONNECTOR 34P HEADER ANGLED	P2, P3
33	7096E3055-84	2	CONNECTOR CL 4P 0.1" ANGLED	P4, P6
34	003-3931-919	1	CONNECTOR CL 6P 0.1" ANGLED	P5
35	0681-0802-06	1	PCB EXTRACTOR	
36				
37				
38				
39				
40				8

Item	Qty.	Dwg./Part no.	Description	Mat'l Spec.	Remarks
Scale 1:1			Date	Remarks USED ON MCS 2000	
Drawn by M R SILVA			8.9.87		
Checked by Pete Piel			22.9.87		
Approved			22.9.87	Finish	

Unless otherwise specified: * Dimensions are in mm., Tolerances on Angles ± 0.5° Holes ± 0.1 Rest ± 0.5

Description: CENTRONICS INTERFACE ASS'Y.

Dwg. no. 7001E9311-19

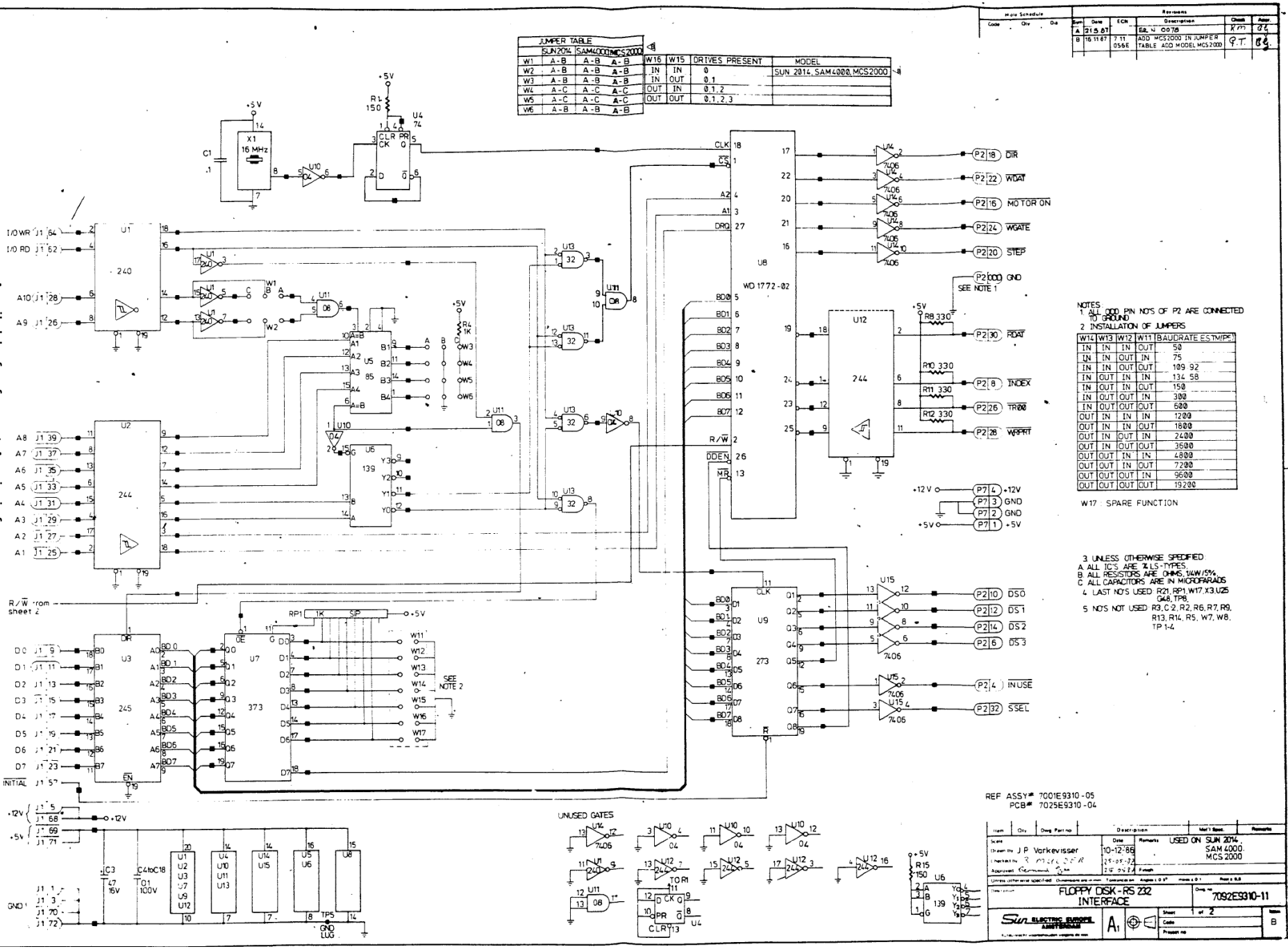
SUN ELECTRIC EUROPE B.V.
Auteursrecht voorbehouden, vrijgens de wet

A2

Sheet 1 of 1
Code
Project no. E-8713

Issue B

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Sym	Date	ECN	Description	Check	Appr
A	21.5.87		ERN 00716		
B	16.11.87	7.11.056E	ADD MCS 2000 IN JUMPER TABLE ADD MODEL NAME		

R/W to sheet 1

P4

P3 17 D0 · P3 16 D1 · P3 15 D2 · P3 2 D3 · P3 3 D4 · P3 4 D5 · P3 5 D6 · P3 6 D7 · P3 8 E · P3 7 VMA · P3 10 RES · P3 11 R/W · P3 23 A1 · P3 22 A2 · P3 21 A3 · P3 20 A4 · P3 24 A5 · P3 19 68D0 · P3 18 IRQ · P3 1 +12VL · P3 13 +5VL · P3 25 GNDL · P3 14 -12VL · P3 9 INT7 · P3 12 IACK7

25 POLE D-CONNECTOR TO CPU-BD J11

U18 20 · U19 14 · U20 08 · U16 6551 ACIA · X2 1.8432MHz · TP7 · X3 1.8432MHz · TP8 · U17 6551 ACIA

R16 1K · +5VL

C35 47µ/16V · C45to45 0.1µ/100V · C34 47µ/16V · C37to44 0.1µ 100V · TP6 GNDLUG · C36 47µ/16V · C47to48 0.1µ/100V · SEE NOTE

JUMPER TABLE			
	SUN 2014	SAM4000	MCS 2000
W9	A-C, B-D	A-C, B-D	A-C, B-D
W10	A-C, B-D	A-C, B-D	A-C, B-D

ESTM RS232C

P5 1 NC · P5 7 RTS · P5 3 DTR · P5 8 RXD · P5 9 TXD · P5 2 DCD · P5 5 DSR · P5 6 CTS · P5 4 GND · P5 10 NC

U21 1488 · U23 1489 · W9 · C19 100p · C20 100p · C21 100p · R19 10K · +12VL · C22 330p · C23 330p · C24 330p · C25 330p

AUX RS232C

P6 7 RTS · P6 3 DTR · P6 8 RXD · P6 9 TXD · P6 2 DCD · P6 5 DSR · P6 6 CTS · P6 4 GND · P6 1 INT · P6 10 NC

U22 1488 · U24 1489 · W10 · C26 100p · C27 100p · C28 100p · R20 10K · +12VL · C29 330p · C30 330p · C31 330p · C32 330p

NOTE
THE CIRCUITRY ON THIS SCHEMATIC IS POWERED BY P3.
+5VL MEANS +5V LOCAL

+5V · R21 1K · U25 74 PR D CLK CLR Q · R17 1K · +5VL · R18 47 · C33 100µ/10V

RES · IACK7 · U20 08

+5VL	+5VL	+5VL	+5VL	+12VL	+5VL	+5VL
U25 74	U20 08	U19 14	U18 20	U21 U22 1488	U23 U24 1489	U16 U17 6551
				-12VL		

UNUSED GATES.

U20 08 · U19 14 · U20 08 · U21 1488 · U20 08 · U22 1488

TO R21

U25 74 PR D CLK CLR Q

Item	Qty	Dwg Part no	Description	Mat Spec	Remarks
Scale			Date	Remarks	USED ON SUN 2014, SAM 4000, MCS 2000
Drawn by J.P. Varkevisser			10-12-86		
Checked by R. MULDER			25-05-87		
Approved Bernard [illegible]			25.05.87		

Unless otherwise specified: [illegible]

FLOPPY DISK-RS 232 INTERFACE

7092E9310-11

Sun ELECTRIC EUROPE AMSTERDAM

A1

Sheet 2 of 2 · Code · Project no · Issue B

REF. ASSY# 7001E9310-05
PCB# 7025E9310-04

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ITEM NO.	QTY.	DWG./PARTNO.	DESCRIPTION	REF.DESIGNATION
1	1	7025E9310-04	PRINTED CIRCUIT BOARD REV.A	
2	1	0681-0802-006	CARD EXTRACTOR	
3	6	0404-2510-523	BOLT M2.5x10 USED WITH ITEM 6,7 & 8	
4	6	0409-2500-103	NUT M2.5 USED WITH ITEM 6,7 & 8	
5				
6	1	3-3931-949	CONNECTOR MALE 34-way RIGHT ANGLE	
7	2	7096E3055-92	CONNECTOR MALE 10-way RIGHT ANGLE	
8	1	7096E3055-84	CONNECTOR MALE 4-way RIGHT ANGLE C.L. 0.1"	
9				
10	4	3-0606-524	TERMINAL POST	
11				
12	1	7076E9311-80	WIRE HARNESS "W1FD" FDC~CPU	
13				
14	90mm	3-0637-611	WIRE TINNED COPPER USED ON ITEM 16	
15	1	7096E2080-22	X-TAL 16MHz	X1.
16	2	7096E2080-23	X-TAL 1.8432MHz	X2,3.
17				
18	1	3-0776-664	IC SOCKET 14 PINS USED ON ITEM 37 & 38.	U21-24.
19	1	3-0776-675	IC SOCKET 28 PINS USED ON ITEM 28 & 34.	U8,16,17.
20				
21	1	0773-7240	INTEGRATED CIRCUIT 74LS240	U1.
22	2	0773-7244	INTEGRATED CIRCUIT 74LS244	U2,12.
23	1	0773-7245	INTEGRATED CIRCUIT 74LS245	U3.
24	2	0773-7074	INTEGRATED CIRCUIT 74LS74	U4,25.
25	1	0773-7085	INTEGRATED CIRCUIT 74LS85	U5.
26	1	0773-7139	INTEGRATED CIRCUIT 74LS139	U6.
27	1	0773-7373	INTEGRATED CIRCUIT 74LS373	U7.
28	1	7096E2080-21	INTEGRATED CIRCUIT WD1772-02	U8.
29	1	0773-7273	INTEGRATED CIRCUIT 74LS273	U9.
30	1	0773-7004	INTEGRATED CIRCUIT 74LS04	U10.
31	2	0773-7008	INTEGRATED CIRCUIT 74LS08	U11,20.
32	1	0773-7032	INTEGRATED CIRCUIT 74LS32	U13.
33	2	0773-0142	INTEGRATED CIRCUIT 7406	U14,15.
34	2	7096E2080-20	INTEGRATED CIRCUIT MC6551	U16,17.
35	1	0773-7020	INTEGRATED CIRCUIT 74LS20	U18.
36	1	0773-7014	INTEGRATED CIRCUIT 74LS14	U19.
37	2	0773-0402	INTEGRATED CIRCUIT MC1488	U21,22.
38	2	0773-0401	INTEGRATED CIRCUIT MC1489	U23,24.
39				
40				
41	6x3/36	7096E3055-05	JUMPER STRIP SINGLE 3-way	W1-6.
42	2x2/36	7096E3055-91	JUMPER STRIP DOUBLE (2-way)	W9,10.
43	1x7/36	7096E3055-91	JUMPER STRIP DOUBLE (7-way)	W11-17.
44	15	7096E3055-12	JUMPER SOCKET	W1-6,9-17.
45				
46				
47	28	0679-1325-000	CAPACITOR 100nF 100V MKMD .4"	C1,4-18,37-48.
48	4	0679-0538	CAPACITOR 47uF 16V TANT.RADIAL	C3,34-36.
49	6	0860-0173-13	CAPACITOR 100pF DISC	C19-21,C26-28.
50	8	0860-0173-18	CAPACITOR 330pF DISC	C22-25,C29-32.
51	1	7096E1055-07	CAPACITOR 100uF 10V TANT.RADIAL	C33.
52				
53				
54	2	0680-2022	RESISTOR 150E 1/4W 5%	R1,15.
55	4	0680-2045	RESISTOR 1K 1/4W 5%	R4,6,17,21.
56	4	0680-2033	RESISTOR 330E 1/4W 5%	R8,10-12.
57	1	0680-2011	RESISTOR 47E 1/4W 5%	R18.
58	2	0680-2075	RESISTOR 10K 1/4W 5%	R19,20.
59	1	7096E0085-07	RESISTOR NETWORK 1K SIP (9x1K)	RP1.
60				
61	1	3-0673-563	LABEL IDENT (7001E9310-05 REV.B)	
62				
63				
64				
65				
66				
67				
68				
69				
70				

Revisions

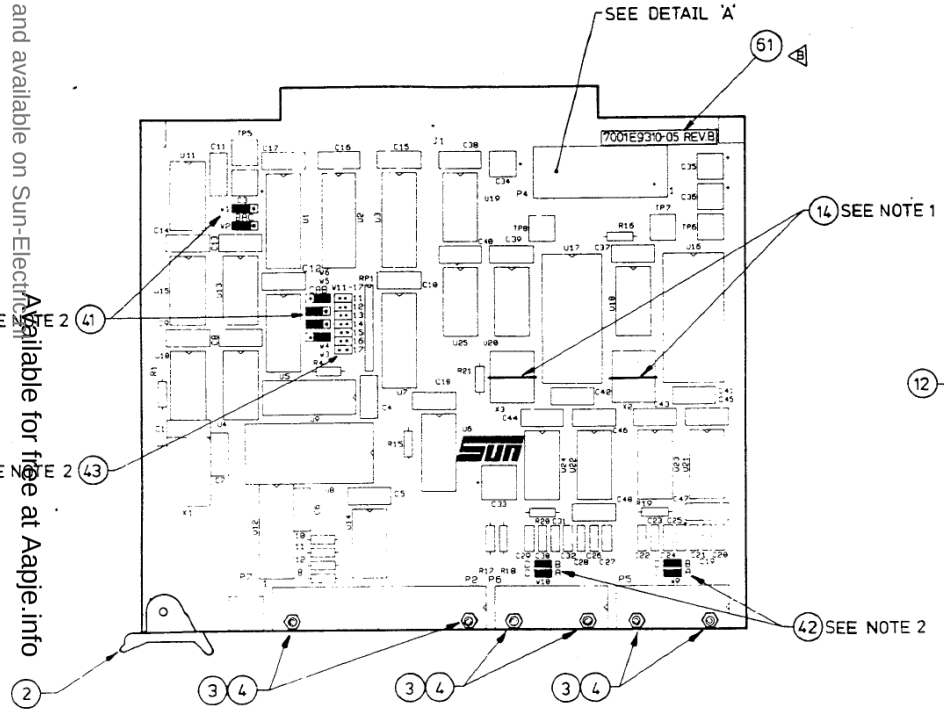
Rev	Date	ECN	Description	Check	Appr
A	210587		ERN# 0078	GT	
B	161187	7.11.056E	CHANG. ITEM 14. ADD. C19-21 & C22-25. ADD. ITEM 61. ADD. MODEL MCS2000.	GT	BG

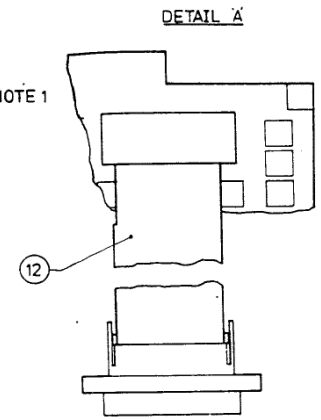
Ref schem. 7092E9310-11	Date	Used in SAM 4000, SUN 2014, MCS 2000.	
Designed by R.MULDER	MAY'87		
Drawn by M.TJIN A SOE	120587		
Checked by			
Description PCB.ASS'Y. FLOPPY DISK/RS232 INTERFACE		Drawing nr 7001E9310-05	
SUN ELECTRIC EUROPE B.V.	A3	Sheet 1 of 2	Issue B

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Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr.
A	21.5.87		ECN #0078	RM	BG
B	16.11.87	711.056E	ADD MCS 2000 IN JUMPER TABLE AND ITEM 61	GT	BG





NOTES: 1. SECURE COMPONENTS X2 AND X3 WITH WIRE ITEM 14 AS SHOWN.

2. POSITION JUMPERS ITEM 44 AS SHOWN ON TABLES BELOW

CIRCUIT REF	JUMPER POSITION
W1	A_B
W2	A_B
W3	A_B
W4	A_C
W5	A_C
W6	A_B
W9	A_C/B_D
W10	A_C/B_D

JUMPER POSITION	MCS 2000 SUN 2014 SAM 4000	
W11	FIT	
W12	FIT	
W13	FIT	
W14	NOT FITTED	
W15	FIT	
W16	FIT	
W17	NOT FITTED	

3. FIT IC SOCKETS ITEM 18 TO POSITIONS U21,22,23 & 24, AND IC SOCKETS ITEM 19 TO POSITIONS U8,16 & 17.

REF SCHEM # 7092E9310_11
PCB # 7025E9310_04

Item	Qty	Dwg Part no	Description	Mat'l Spec	Remarks

Scale N.T.S.
Drawn by R. SILVA
Checked by
Approved
Date 13/5/87
Remarks USED ON SUN 2014/ SAM 4000/MCS 2000
Finish

Unless otherwise specified

PCB ASSY
FLOPPY DISK / RS 232 INTERFACE

7001E9310_05

Sun

A2

Sheet 2 of 2

Issue B

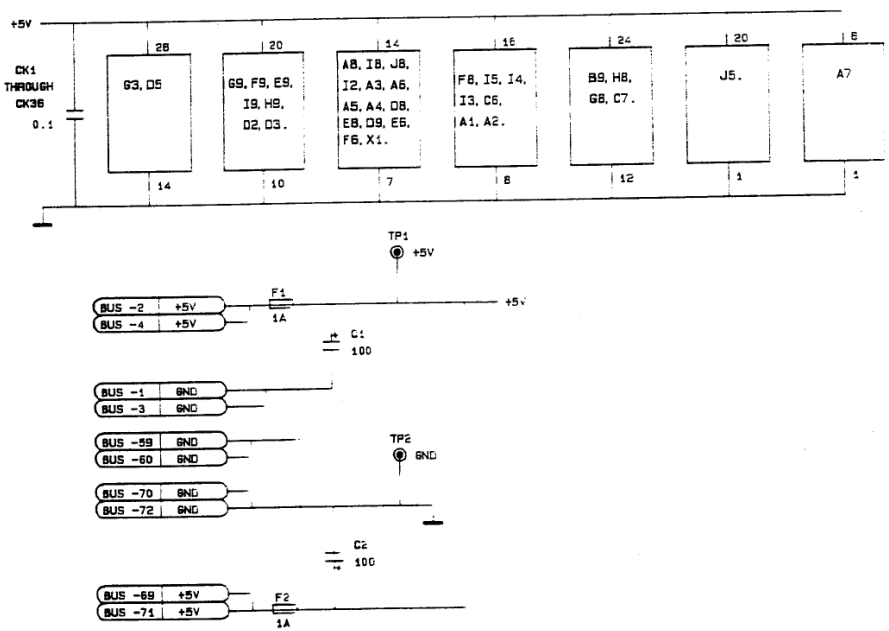
Archived and available on Sun-Electric.nl
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Revisions					
Rev	Date	ECN	Description	Check	Appr
A	02-89		ERN# 0315	EK	EB
B	04'89	4.01.018E	CHANGED PAL'S TO GAL'S. DELETED SHT 6OF6, PAL-LISTINGS	03	BB

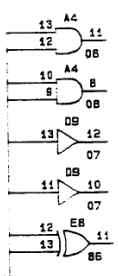
BUS CONNECTOR					
PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	GND	25	BA1	49	/INT6
2	+5V	26	BA9	50	/MEMEN
3	GND	27	BA2	51	/INT5
4	+5V	28	BA10	52	/INT3
5	+12V	29	BA3	53	/INT4
6	-12V	30	BA11	54	/INT2
7	TRSCOPE	31	BA4	55	NC
8	TRSCOPE	32	BA12	56	NC
9	BD0	33	BA5	57	/INIT
10	BD8	34	BA13	58	READY
11	BD1	35	BA6	59	GND
12	BD9	36	BA14	60	GND
13	BD2	37	BA7	61	MEMRD
14	BD10	38	BA15	62	IORD
15	BD3	39	BA8	63	MEMWR
16	BD11	40	BA16	64	IOWR
17	BD4	41	HS OUT	65	/BLDS
18	BD12	42	BA17	66	NC
19	BD5	43	VS OUT	67	-12V
20	BD13	44	BR/W	68	+12V
21	BD6	45	TTL VIDEO	69	+5V
22	BD14	46	BA21	70	GND
23	BD7	47	COMP VIDEO	71	+5V
24	BD15	48	NC	72	GND

P2 PANDUIT 5 MALE	
PIN NO.	SIGNAL
1	HS SCOPE
2	DOTCLK 6
3	NC
4	/VS SCOPE
5	/SCOPE VIDEO

POWER CONNECTIONS:



SPARES :



NOTES:

1/ UNLESS OTHERWISE SPECIFIED:
- A/ ALL RESISTORS ARE IN OHMS, 1/4W, 5%
- B/ ALL CAPACITORS ARE IN MICRO-FARADS
- C/ ALL DIODES ARE 1N914 OR 1N4148
- D/ ALL IC'S ARE 74LS-SERIES TYPE
- E/ ALL POLARIZED CAPACITORS ARE 16V

2/ LAST USED NO'S: R16, C8, CK36, L1, LED2, T1, TP2.

3/ NOT USED NO'S:

4/ JUMPERSETTINGS :

- W1 : DEFAULT NOT INSTALLED
  8K RAM
- W2 : DEFAULT NOT INSTALLED
  50Hz
- W3 : DEFAULT 2-3 IN COPPER
- W4 : DEFAULT 2-3 IN COPPER
- W5 : DEFAULT 2-3 IN COPPER
- W6 : DEFAULT INSTALLED
  POSITIVE HS OUT
- W7 : DEFAULT INSTALLED
  POSITIVE VS OUT

Ref. pcb 7025E9310-59		Used in	MCS 2000
Ref assy 7001E9311-59	Date		
Designed by MARO AMATER	11-88		
Drawn by H.v/d KIBBOOM	88-88	Remarks	POWER DISTRIBUTION
Checked by E.VDK.			
Approved	7.89		
Description SCHEMATIC ECAT		Drawing nr	7092E9311-65
BSM ELECTRIC EUROPE B.V.	A3	Sheet 1 of 5	Issue B
		Project nr E8815	

Archived

SIGNAL WHERE USED LIST

NAME	GENERATED (SHT-GRID)	USED (SHT-GRID)
A0	3-D7	4-D8, C7.
A1	3-D7	4-D6
A2	3-D7	4-D6
A3	3-D7	4-D6
A4	3-D7	4-C6
A5	3-C7	4-C6
A6	3-C7	4-C6
A7	3-C7	4-C6
A8	3-C7	4-B6
A9	3-C7	4-B6
A10	3-C7	4-B6
A11	3-C7	4-B6
A12	3-C7	4-B6
A13	NOT USED	NOT USED
A14	NOT USED	NOT USED
A15	3-B7	3-E7
BA0	3-D8	3-D7
BA1	3-D8	3-D7
BA2	3-D8	3-D7
BA3	3-D8	3-D7
BA4	3-C8	3-C7
BA5	3-C8	3-C7
BA6	3-C8	3-C7
BA7	3-C8	3-C7
BA8	3-C8	3-C7
BA9	3-C8	3-C7
BA10	3-C8	3-C7
BA11	3-C8	3-C7
BA12	3-C8	3-C7
BA13	3-C8	3-C7
BA14	3-B8	3-B7
BA15	3-B8	3-B7
BA16	3-B8	3-B7
BA17	NOT USED	NOT USED
BA18	NOT USED	NOT USED
BA19	NOT USED	NOT USED
BA20	NOT USED	NOT USED
BA21	3-E8	3-E7
BABCLK	3-F4	3-F5; 5-E6, D6.
BABDATA	5-E6	5-D4; 3-D2.
BD0	3-E8	3-E7
BD1	3-E8	3-E7
BD2	3-E8	3-E7
BD3	3-D8	3-D7
BD4	3-D8	3-D7
BD5	3-D8	3-D7
BD6	3-D8	3-D7
BD7	3-D8	3-D7
BIT7CH0	5-F6	5-D4; 3-D2.
/BLDS	3-F8	3-F7.
BLINK	5-B6	5-C4.
BLINKEN	5-A7	5-B4.
BR/W	3-B8	3-B7.
CD	4-D1	5-C4.
CHAR0.0	5-A4	5-A7.
CHARCLK	3-D2	3-E7, F8, F3, F2; 4-D7, C4.
CHARINV	4-C2	4-D1.
CHS0	3-A7	3-A8; 4-C2.
CHS1	3-A7	3-A8; 4-C2.
CHS2	3-A7	3-A8; 4-C2.
/CLRBARCRT	3-D2	3-F4; 5-F7.
/CLRBR	5-B4	4-D1.
COMP VIDEO	5-C1	5-C2.
/CPUACC	3-F7	3-B2; 4-E6, D6, C6.
/CPUSTD	3-F5	3-F7, E7, C2.
/CPUREQ	3-F7	3-F6, C2.
/CSCRTC	3-F7	4-D7.
/CSRAM	3-C2	4-D4.
CUSYN	4-B7	5-C4.

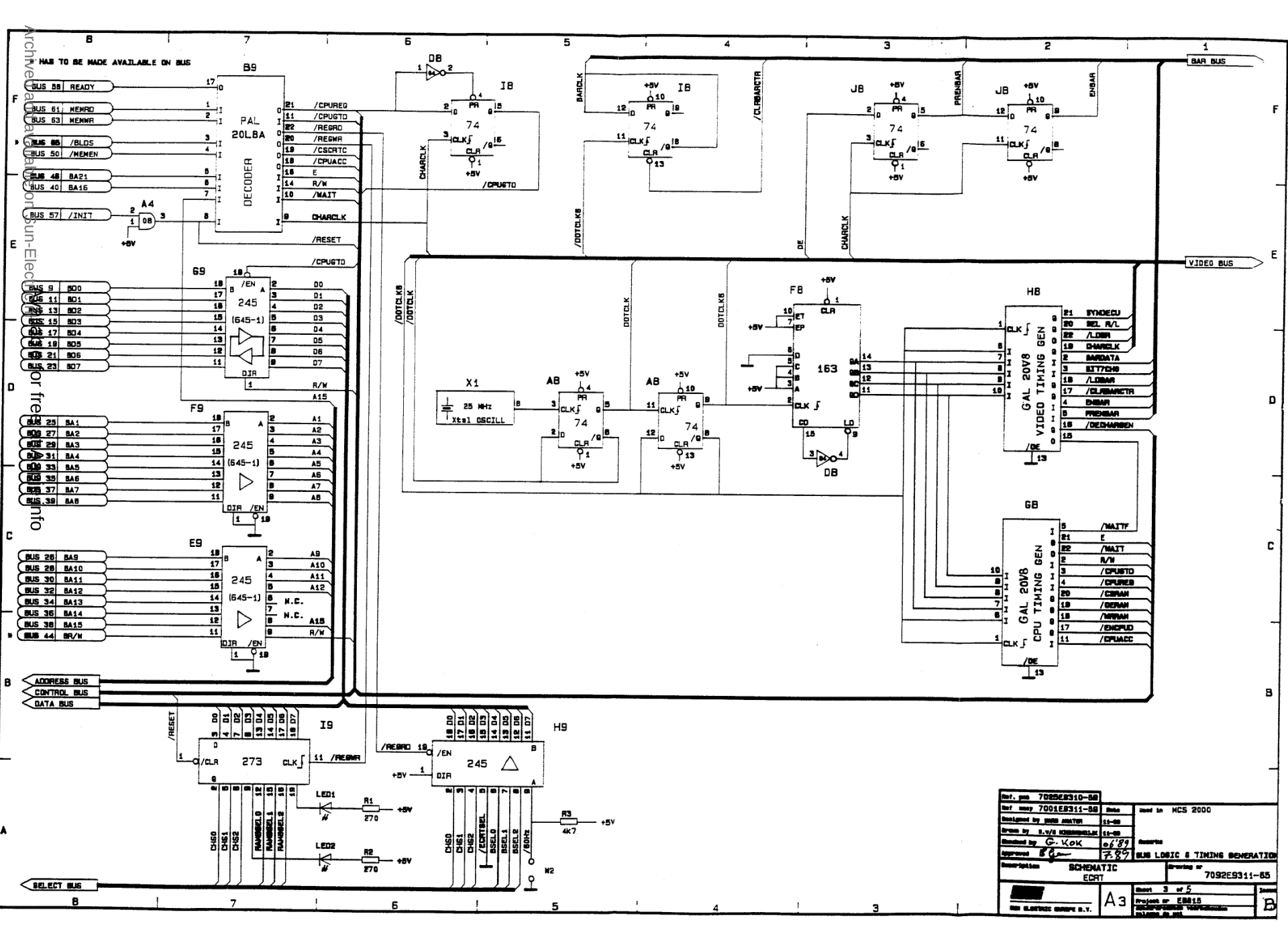
SIGNAL WHERE USED LIST

NAME	GENERATED (SHT-GRID)	USED (SHT-GRID)
D0	3-E7	3-B7, B6; 4-E7, E5.
D1	3-E7	3-B7, B6; 4-E7, E5.
D2	3-E7	3-B7, B6; 4-E7, E5.
D3	3-D7	3-B7, B5; 4-E7, E5
D4	3-D7	3-B7, B5; 4-E7, E5
D5	3-D7	3-B7, B5; 4-E7, E5
D6	3-D7	3-B7, B5; 4-E7, E5
D7	3-D7	3-B7, B5; 4-E7, E5
DE	4-C7	3-F3.
DESYN	4-B7	5-A4, C4.
DIGVIDEO	5-C4	5-C3.
/DIGVIDEO	5-C4	5-C2.
DOTCLK	3-D5	3-D4; 4-C1.
/DOTCLK	3-D5	3-D5; 5-C4.
DOTCLK6	3-D4	3-D4; 5-E5, E1.
/DOTCLK6	3-D4	3-D2, B2, F5.
E	3-C2	3-F7, 4-E7.
/ECRTSEL	3-A5	3-A5.
ENBAR	3-F2	3-D2; 5-C4.
/ENCPUD	3-B2	4-E5.
HS	4-D7	5-B4, E5, E4, F3.
HS OUT	5-F2	5-F1.
HS SCOPE	5-E5	5-D1.
/INIT	3-E8	3-E8.
INV	5-B6	5-B4; 4-D3.
/LDBAR	3-D2	5-E7, D7.
/LDSR	3-D2	4-C1.
LVD0	4-D3	4-D2; 5-D7.
LVD1	4-D3	4-D2; 5-D7.
LVD2	4-D3	4-D2; 5-D7.
LVD3	4-D3	4-D2; 5-D7.
LVD4	4-D3	4-D2; 5-E7.
LVD5	4-D3	4-D2; 5-E7.
LVD6	4-D3	4-D3; 5-E7, C7, A7.
LVD7	4-D3	4-C3; 5-E7, B6.
MA0	4-E7	4-E6.
MA1	4-E7	4-E6.
MA2	4-D7	4-E6.
MA3	4-D7	4-E6.
MA4	4-D7	4-D6.
MA5	4-D7	4-D6.
MA6	4-D7	4-C6.
MA7	4-D7	4-C6.
MA8	4-D7	4-C6.
MA9	4-D7	4-C6.
MA10	4-D7	4-B6.
MA11	4-D7	4-B6.
/MEMEN	3-F8	3-F7.
MEMRD	3-F8	3-F7.
MEMWR	3-F8	3-F7.
/OECHARGEN	3-D2	4-E2.
/OERAM	3-C2	4-D4.
OPTION	5-C6	5-C4.
PD0	4-D2	4-D2.
PD1	4-D2	4-D2.
PD2	4-D2	4-D2.
PD3	4-D2	4-D2.
PD4	4-D2	4-D2.
PD5	4-D2	4-D2.
PD6	4-D2	4-D2.
PD7	4-D2	4-D2.
PRENBAR	3-F3	3-D2.

SIGNAL WHERE USED LIST

NAME	GENERATED (SHT-GRID)	USED (SHT-GRID)
RA0	4-E7	4-D2; 5-B5.
RA1	4-E7	4-D2; 5-B5.
RA2	4-E7	4-D2; 5-C5.
RA3	4-E7	4-D2; 5-C5.
RAMBSEL0	3-A7	3-A5; 4-C5.
RAMBSEL1	3-A7	3-A5; 4-C5.
RAMBSEL2	3-A7	3-A5; 4-C5.
READY	3-F8	3-F7.
/REGRD	3-F7	3-B6.
/REGWR	3-F7	3-B7.
/RESET	3-E8	3-B7; 4-D7.
R/W	3-B7	3-E7, D7, C2; 4-D7, E5.
/SCOPE VIDEO	5-E1	5-C4.
SEL R/L	3-E2	4-C2.
SYNDECU	3-E2	4-B7, C7; 5-C7.
TTL VIDEO	5-C2	5-C1.
VA0	4-E6	4-D5.
VA1	4-E6	4-D5.
VA2	4-E6	4-D5.
VA3	4-E6	4-D5.
VA4	4-C6	4-D5.
VA5	4-C6	4-D5.
VA6	4-C6	4-D5.
VA7	4-C6	4-D5.
VA8	4-B6	4-D5.
VA9	4-B6	4-D5.
VA10	4-B6	4-D5.
VA11	4-B6	4-D5.
VD0	4-D4	4-D4, E4.
VD1	4-D4	4-D4, E4.
VD2	4-D4	4-D4, E4.
VD3	4-D4	4-D4, E4.
VD4	4-D4	4-D4, E4.
VD5	4-D4	4-D4, E4.
VD6	4-D4	4-D4, E4.
VD7	4-D4	4-D4, E4.
VS	4-D7	5-A5, B4, B6, C4, E4, F3.
/VS	5-A5	5-A4.
VS OUT	5-F2	5-F1.
/VS SCOPE	5-D2	5-D1.
/WAIT	3-C2	3-E7.
/WAITF	3-D2	3-C2.
/WRRAM	3-B2	4-D4.

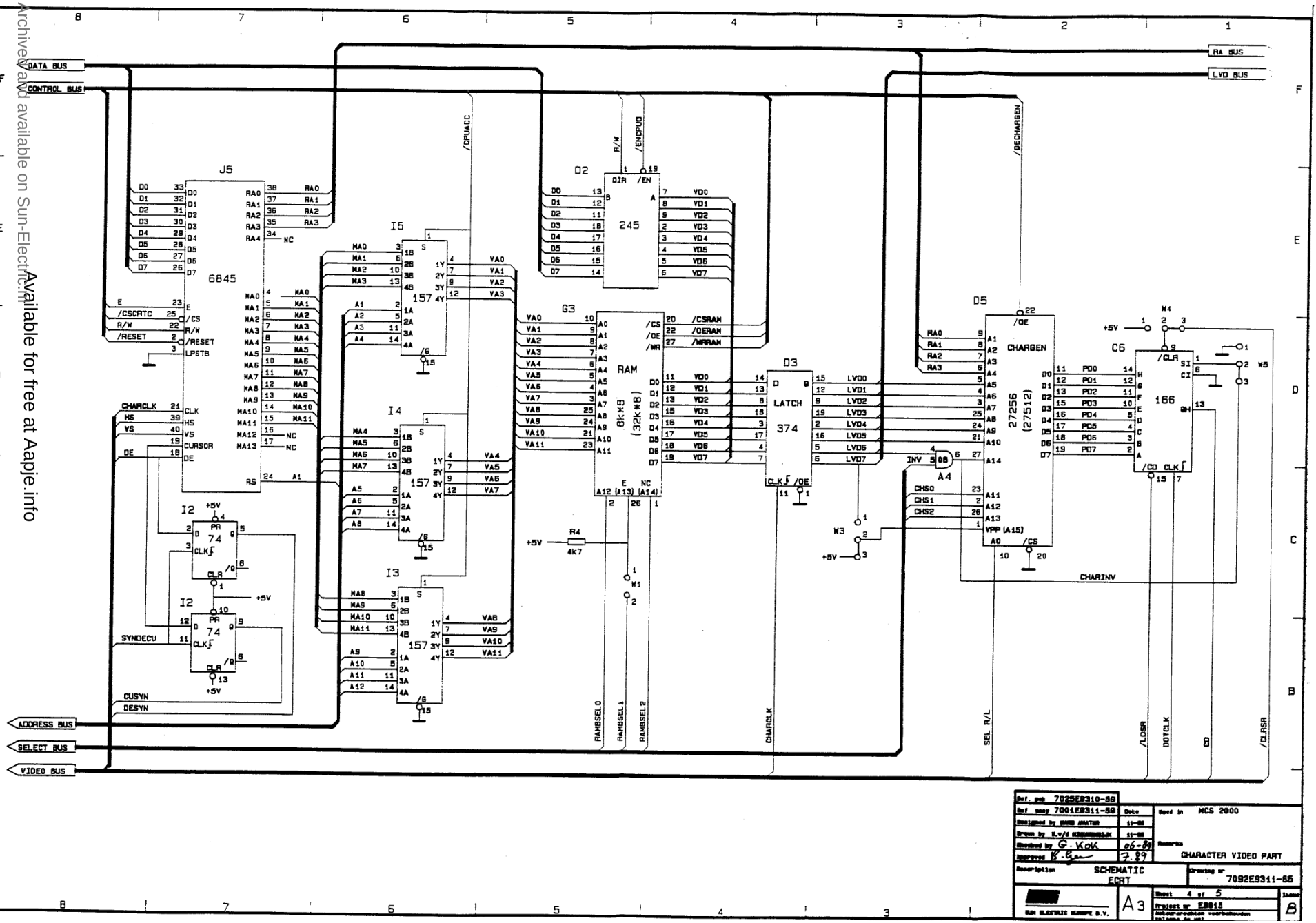
Ref. pcb	7025E9310-50		
Ref assy	7001E9311-50	Date	Used in NCS 2000
Designed by	NARD AMATER	11-88	
Drawn by	M.TJIN A SOE	280489	
Checked by	G. WOK.	0689	Remarks :
Approved		7.89	SIGNAL WHERE USED LISTING
Description	SCHEMATIC ECRT		Drawing nr 7092E9311-65
[redacted] NEC ELECTRONICS EUROPE B.V.	A3	Sheet 2 of 5	Issue B
		Project nr E9311	



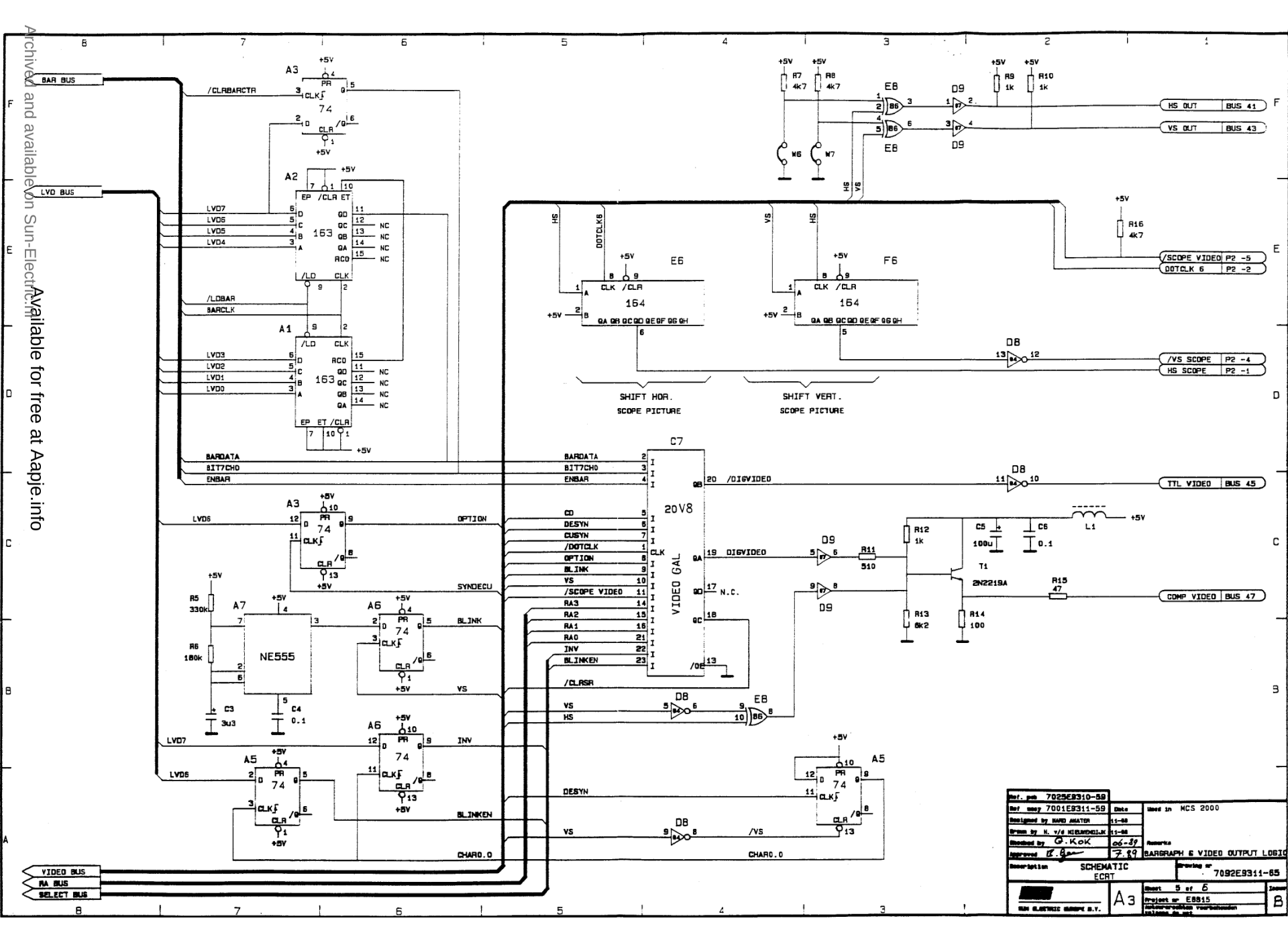
Ref. pos	7005E9310-58
Ref assy	7001E9311-58
Designed by	
Drawn by	
Checked by	G. Kok 01'89
Approved	7.89
Used in	MCS 2000
Remarks	BUS LOGIC & TIMING GENERATION
Description	SCHEMATIC ECRT
Drawing nr	7092E9311-65
Sheet	3 of 5
Project nr	E9815
Size	A3
Issue	B

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Ref. pcb 7025E9310-58		Used in MCS 2000	
Ref assy 7001E8311-58	Date		
Designed by [redacted]	11-88		
Drawn by [redacted]	11-88		
Checked by G. Kok	06-89	Remarks	
Approved [redacted]	7.89	CHARACTER VIDEO PART	
Description SCHEMATIC ECRT		Drawing nr 7092E9311-65	
[redacted] SUN ELECTRIC EUROPE B.V.	A3	Sheet 4 of 5	Issue B
		Project nr E8815	
		Information reproduction prohibited by law	

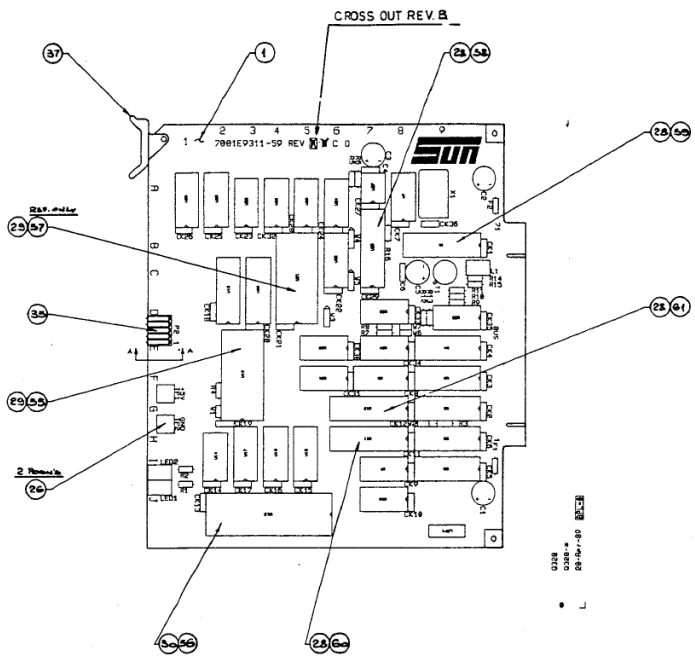


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Ref. pcb 7025E9310-59			
Ref assy 7001E9311-59	Date	Used in MCS 2000	
Designed by HARD AMATER	11-88		
Drawn by H. v/d KIEBOOMDIJK	11-88		
Checked by G.KOK	06-89	Remarks	
Approved	7.89	BARGRAPH & VIDEO OUTPUT LOGIC	
Description SCHEMATIC ECAT		Drawing nr 7002E9311-65	
SUN ELECTRIC EUROPE B.V.	A3	Sheet 5 of 6	Issue B
		Project nr E8815	

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Rev	Date	ECN	Remarks: Description	Check	Appr
A	APRIL '90	—	GAL'S 0.2.5	G.K.	BJ
B	10-90	0.10.085E	ITEM 35 WAS 4N2-N43-05		BJ
C	04-94	4.01.018E	CHANGED PAL'S TO GAL'S.		BJ



LINE NR	DIRECT ASSEM PART NR.	QUANT	COMPONENTS & SUB ASSEMBLIES	ITEM NR.
1	7025E9310-59	1	ECRT PCB	
2				
3	0680-2011-00	1	RESISTOR 47E WW 5%	R15
4	0680-2018-00	1	RESISTOR 100E WW 5%	R14
5	0680-2030-00	2	RESISTOR 270E WW 5%	R1, R2
6	0680-2038-00	1	RESISTOR 510E WW 5%	R11
7	0680-2045-00	3	RESISTOR 1K WW 5%	R9, R10, R12
8	0680-2067-00	5	RESISTOR 4K7 WW 5%	R3, R4, R7, R8, R16
9				
10	0680-2070-00	1	RESISTOR 6K2 WW 5%	R13
11	0680-2113-00	1	RESISTOR 180K WW 5%	R6
12	0680-2119-00	1	RESISTOR 330K WW 5%	R5
13				
14	7096E1055-13	3	CAPACITOR 100µF 16V TANTALUM	C1, C2, C5
15	7096E1080-13	38	CAPACITOR 0.1µF 63V CERAMIC	C4, C6, C31-36
16	0679-0449-00	1	CAPACITOR 3.3µF 20V TANTALUM	C3
17				
18	7096E2055-14	1	LED YELLOW RA HLMP 5040	LED 1
19	7096E2055-13	1	LED GREEN RA HLMP 5050	LED 2
20	7096E2055-26	1	TRANSISTOR 2N2219	T1
21	0176-0912-00	1	TRANSISTOR PAD	T1
22	7096E2080-44	1	CRYSTAL OSCILLATOR 25MHz	X1
23				
24	0719-0106-07	2	PICO FUSE 1A	F1, F2
25	7096E4055-65	1	CHOKE 882114-3-A4	L1
26	0536-0302-00	2	TEST POINTS	TP1, TP2
27				
28	7096E3056-05	4	IC SOCKET 24-WAY	C7, B9, G8, H8
29	7096E3056-07	2	IC SOCKET 28-WAY	D5, G3
30	7096E3056-08	1	IC SOCKET 40-WAY	J5
31				
32	7096E3055-05	4	JUMPER STRIP 2-WAY 1 MAKES 18	W1, W2, W6, W7
33	7096E3055-05	3	JUMPER STRIP 3-WAY 1 MAKES 12	W3, W4, W5
34	7096E3055-12	3	JUMPER	W1, W6, W7
35	4162-1678-04	1	CONNECTOR MTA 5-WAY RA	P2
36				
37	0681-0802-06	1	CARD EXTRACTOR	
38				
39				
40				
41	0773-0528-00	1	IC LM 555	A7
42	0773-7007-00	1	IC 7407	D9
43	0773-7004-00	1	IC 74LS04	D8
44	0773-7008-00	1	IC 74LS08	A4
45	0773-7074-00	7	IC 74LS74	A3, A5, A6, A8, I2, I8, J8
46				
47	0773-7086-00	1	IC 74LS86	H8
48	0773-7157-00	3	IC 74LS157	I3, I4, I5
49	0773-7163-00	3	IC 74LS163	A1, A2, F8
50	0773-7164-00	2	IC 74LS164	H6, F6
51	0773-7166-00	1	IC 74LS166	C6
52	0773-7245-00	5	IC 74LS245	B9,F9,G9, H9,D2
53	0773-7273-00	1	IC 74LS273	I9
54	0773-7374-00	1	IC 74LS374	D3
55	7096E2080-26	1	IC RAM 8K * 8	G3
56	7096E2080-30	1	IC 68B45SP	J5
57	0703E0050*-01	1	EPROM PROGRAMMED	D5, SEE NOTE
58	0733E0035*-64	1	VIDEO GAL	C7
59	0733E0036*-64	1	DECODER GAL	B9
60	0733E0037*-64	1	VIDEO TIMING GENERATOR GAL	H8
61	0733E0038*-64	1	CPU TIMING GENERATOR GAL	G8
62				
63				
64				
65	7092E9311-65	1	SCHEMATIC	REF. ONLY
66	0692E9306-08	1	FUNCTIONAL DESCRIPTION	REF. ONLY
67				
68				
69				
70				
71			NOTE : * = 1 or up	
72				
73				
74				
75				
76				
77				
78				
79				
80				

Item	Qty	Dwg / Part no	Description	Remarks
Scale 1:1			Date	Used on Mac 2000
Designed by G.Kok.				Material
Drawn by M. Tjin A Sjoe			18.06.89	
Checked by R.Lammers				
Approved			6.7.89	Finish

Unless otherwise specified: Dimensions are in mm Tolerances on Angles ± 0.5 Holes ± 0.1 Rest ± 0.5

Remove all sharp corners and remove burrs

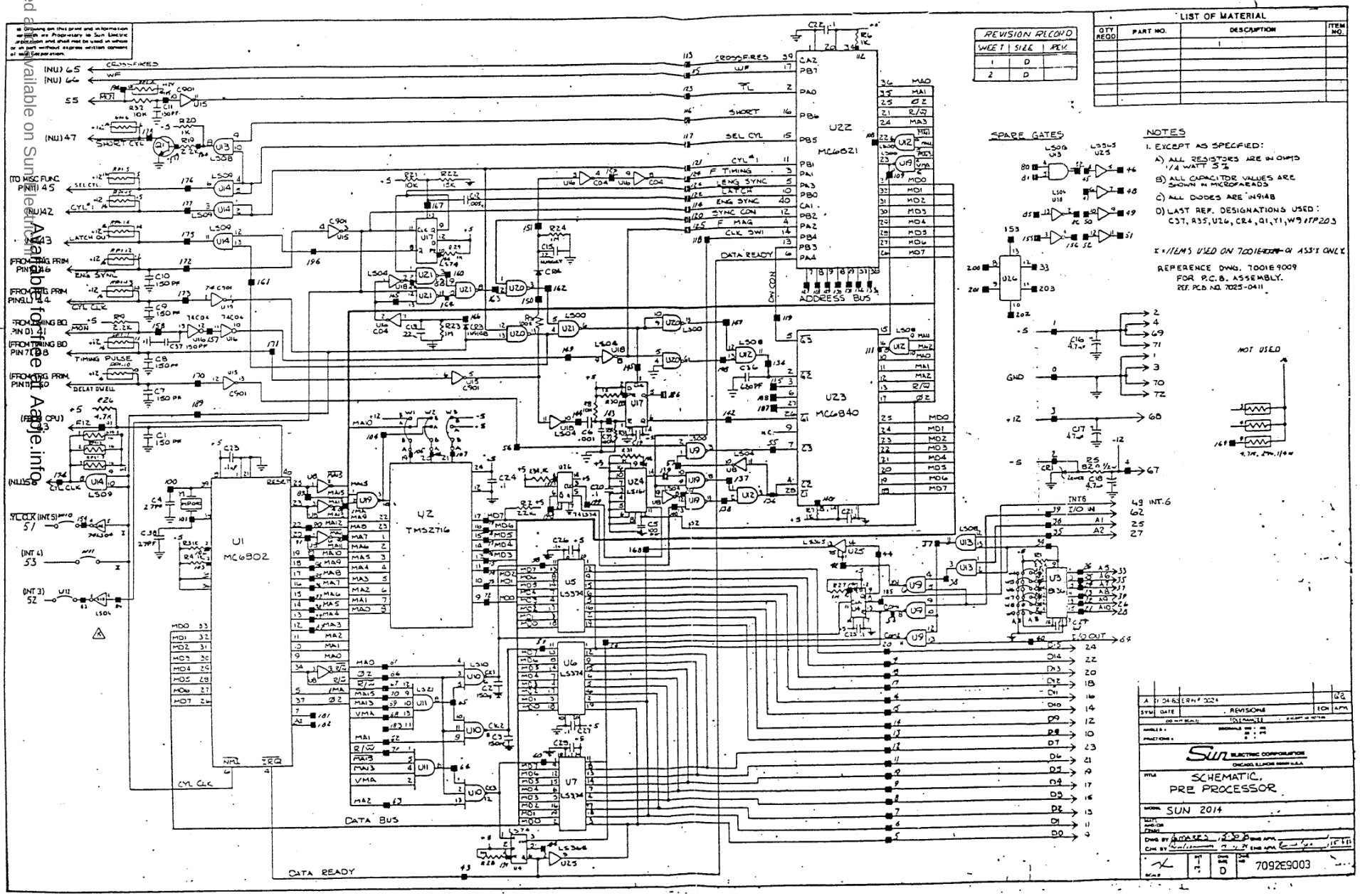
Description: PRINTER CIRCUIT BOARD ASS'Y ECRT

Dwg no 7001E9311-59

Sun Microsystems, Inc. Mountain View, California

A1 | Sheet 1 of 1 | Code | Project no 6-5516 | Size C

Archived document available on Sunhelp.Aaabbb.info

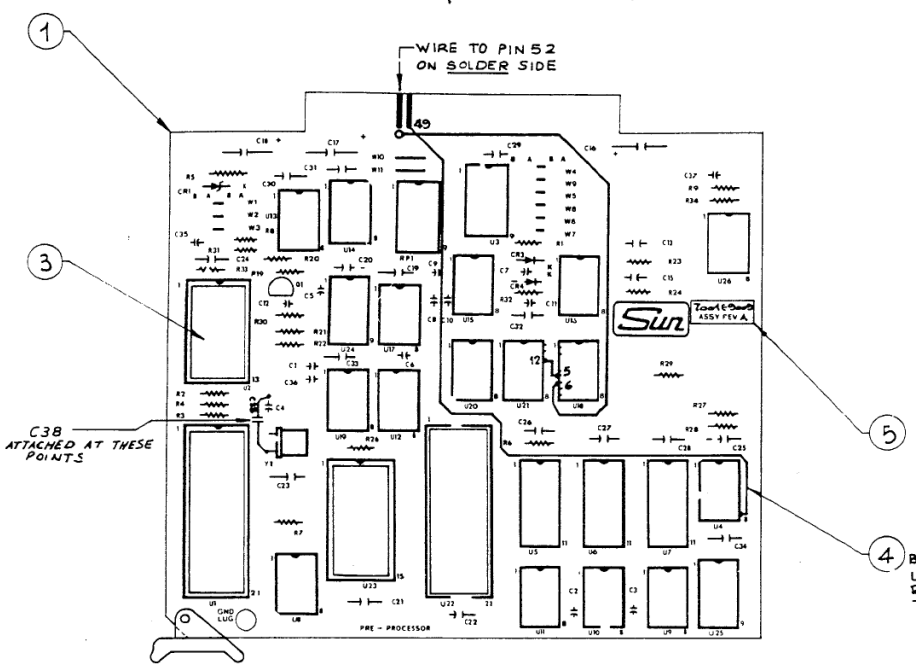


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Hole Schedule		
Code	Qty	Dia

Revisions					
Sym	Date	ECN	Description	Check	Appr.
A	07.10.87		FRN# 0109	P.T.	BJ

COMPONENT-SIDE (LEGEND)



NOTES:

1. REMOVE U2.

5	1	3.0673.563	LABEL IDENT (7001E9009 Rev.A)	
4	230mm	0664-2422	WIRE 24 AWG	
3	1	7056E2091-50	EPROM PROGRAMMED (PRE-PROC. 2Gyl)	U2
2				
1	1	7001-0390	PCB ASS'Y PREPROCESSOR REV C	
Item	Qty	Part No.	Description	Remarks

Scale	N.T.S.	Date	Remarks: SUN 2014, SAM 4000, MCS 2000.
Drawn by	Tjin A Sor M.	29-10-87	
Checked by	Peter Tel	11.05.88	
Approved	Bernard Zee	17.5.88	

PRINTED CIRCUIT BOARD ASS'Y
PRE-PROCESSOR

7001E9009

Sun

A2

Sheet 1 of 1

Issue A

B-B	B-B	B-B	B-B	A-A	A-A	B-B	A-A	A-A	Req'd	Req'd
W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11

JUMPER LOCATION TABLE

REF B/M# 0608C/5A
REF. MOD. INSTR.# 0692E9505-74
REF. PCB# 7025-0411 REV. M
REF. SCHEM# 7092E9003

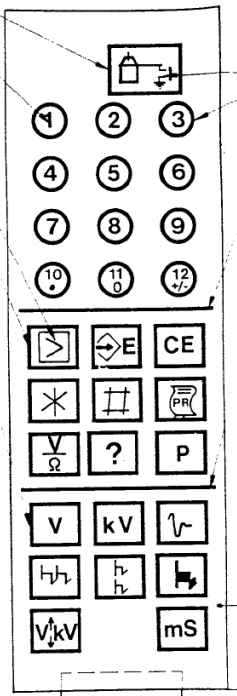
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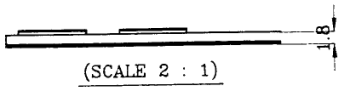
Revisions					
Rev	Date	ECN	Description	Check	Appr
B	9'91		ECN 109.089E REDRAWN AND NEW SCREENING DWG.	D.V.	BG.

SILVER PER SUN COLOUR CHIP
NO: 3551-0702
(ALL RECTANGULAR BORDERS, ALL LETTERING EXCEPT ENGINE KILL SYMBOL)

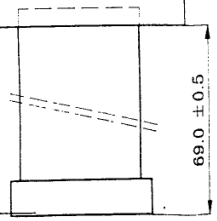
RED PER SUN COLOUR CHIP
NO: 3551-0204
(2 LINES,"ENGINE KILL" SYMBOL, ALL CIRCULAR BORDERS)

BLACK BACKGROUND PER SUN COLOUR CHIP NO: 3551-0103





(SCALE 2 : 1)



BERG CONNECTOR

SPECIFICATIONS :

GENERAL DESCRIPTION
30 POSITION TACTILE DOME MEMBRANE KEYBOARD WITH PRINTED EMI/RFI SHIELD.

OVERLAY MATERIAL
FACEPLATE TO BE TACTILE EMBOSSED MATT MAR-RESISTANT POLYESTER WITH 3 COLOURS.

SHIELDING
A FULL METALLIC SHIELD SHALL BE PROVIDED UNDER OVERLAY MATERIAL AND TERMINATED AT PIN 13.

DOMES
HEAT EMBOSSED IN POLYESTER OVERLAY.

BACKING STIFFENER
KEYBOARD TO BE MOUNTED TO 20 MIL LEXAN (PC) STIFFENER.

ADHESIVE: FASSON 112E ADHESIVE TAPE
ADHESIVE SHALL COVER THE ENTIRE BACKING EXCEPT FOR AN AREA OF 0.6 mm AROUND THE PERIMETER. ENTIRE AREA COVERED BY EASILY REMOVEABLE RELEASE LINER.

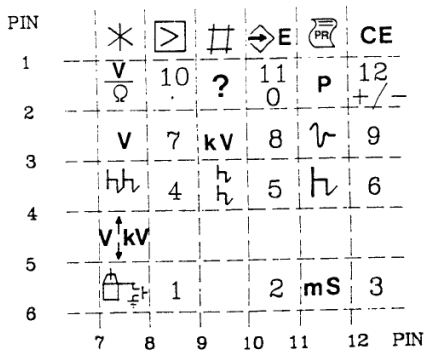
TAIL AND TERMINATION
TAIL WITH PRINTED DIELECTRIC FLEXTAIL COVER. BERG 65801-013 CONNECTOR TO BE USED FOR TERMINATION OF ALL 13 CONTACTS.

SWITCH CHARACTERISTICS

CONTACT RESISTANCE (CLOSED)	100 OHMS (MAXIMUM)
CONTACT BOUNCE	20 MSEC (MAXIMUM)
CURRENT RATING	20 MA@ 30VDC (MAXIMUM)
LIFE	3 MILLION OPERATIONS

WILL RETURN TO THE OPEN POSITION WITHIN 0.1 SEC AFTER BEING CLOSED CONTINUOUSLY FOR 1 MIN.

OUTPUT
OUTPUT CONNECTOR WILL BE BERG P/N 65801-013



NOTE :

KEY LOCATION AND SCREENING DETAILS SEE DWG. 7030E9302-54 (2 SHEETS).

SUPPLIER DIAMOND H. CONTROLS LIMITED.

Item	Qty.	Dwg./Part no	Description		Remarks
Scale	1 : 1 (2 : 1)		Date	Used in	MEA-1500 SL
Designed by	D.V.		9'91		
Drawn by	D.V.		9'91	Material	SEE DRAWING
Checked by	D.V.		9'91		
Approved			16. 9. 91	Finish	

Unless otherwise specified: Dimensions are in mm; Tolerances on: Angles ± 0.5, Holes ± 0.1, Rest ± 0.5

Remove all sharp corners and remove burrs

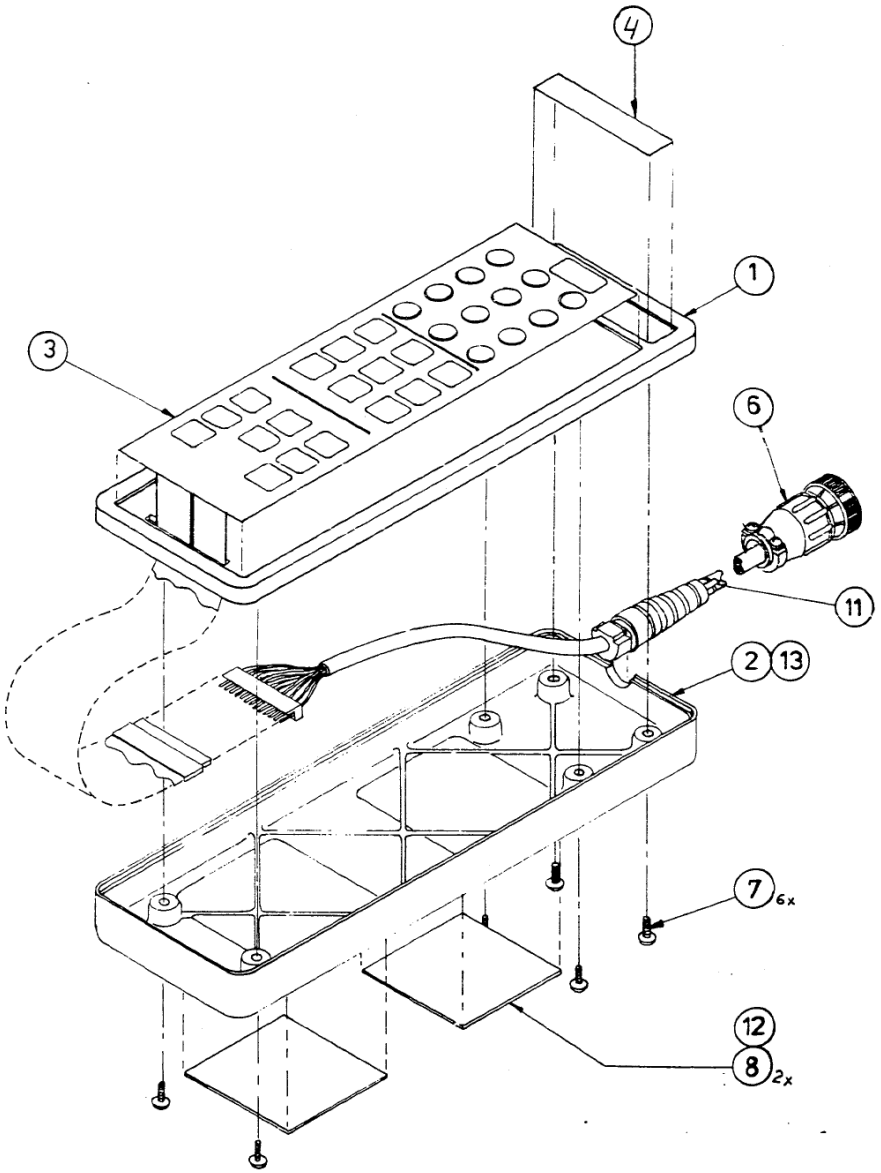
Description	Dwg no	Issue
KEYPAD, REMOTE CONTROL	7010E9310-83	B

SUNELECTRIC B.V.
Auteursrecht voorbehouden volgens de wet

A2 | Sheet of | Code | Project no.

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Rev	Date	Description	Check	Appr.
A	09-'91	ERN #0607 REL. FOR PROD.	P.T.	



NOTES:

1. PLACE ASSEMBLED REMOTE IN BUBBLE BAG, ITEM 9, AND SECURE WITH TAPE ITEM 10.
2. APPLY ITEM 13 TO RECESSED AREA IN ITEM 2 (MAGNET RECESS). APPLY ITEM 12 TO ITEM 8 AND PRESS INTO MAGNET RECESS. DO NOT OVER APPLY ITEM 12/ AVOID EXCESS ADHESIVE AROUND EDGES OF MAGNET.
3. WRITE ON CABLE MARKER (ITEM 11) PIN "7009E9316-54 REV. A"

Item	Qty.	Dwg./Part no	Description	Remarks
13	A/R	0626.0065	ACTIVATOR	
12	A/R	0626.0026	ADHESIVE	
11	1	5878.0013	CABLE MARKER	
10	A/R	0681.0109	MASKING TAPE, 1"	
9	1	0671.0627	BAG, BUBBLE (7"x9")	
8	2	0865.0112	TAPE, MAGNETIC (2"x2")	
7	6	0403.1361.06	SCREW, 6-32x 3/8 R.H.	
6	1	6004E9311-22	CABLE ASS'Y II, REMOTE CONTROL	
5				
4	1	4600E9309.89	MCS. INSERT LABEL	
3	1	7010E9310.83	KEYPAD REMOTE CONTROL	
2	1	7054.0103	REMOTE CASE LOWER	
1	1	7054.0102	REMOTE CASE UPPER	

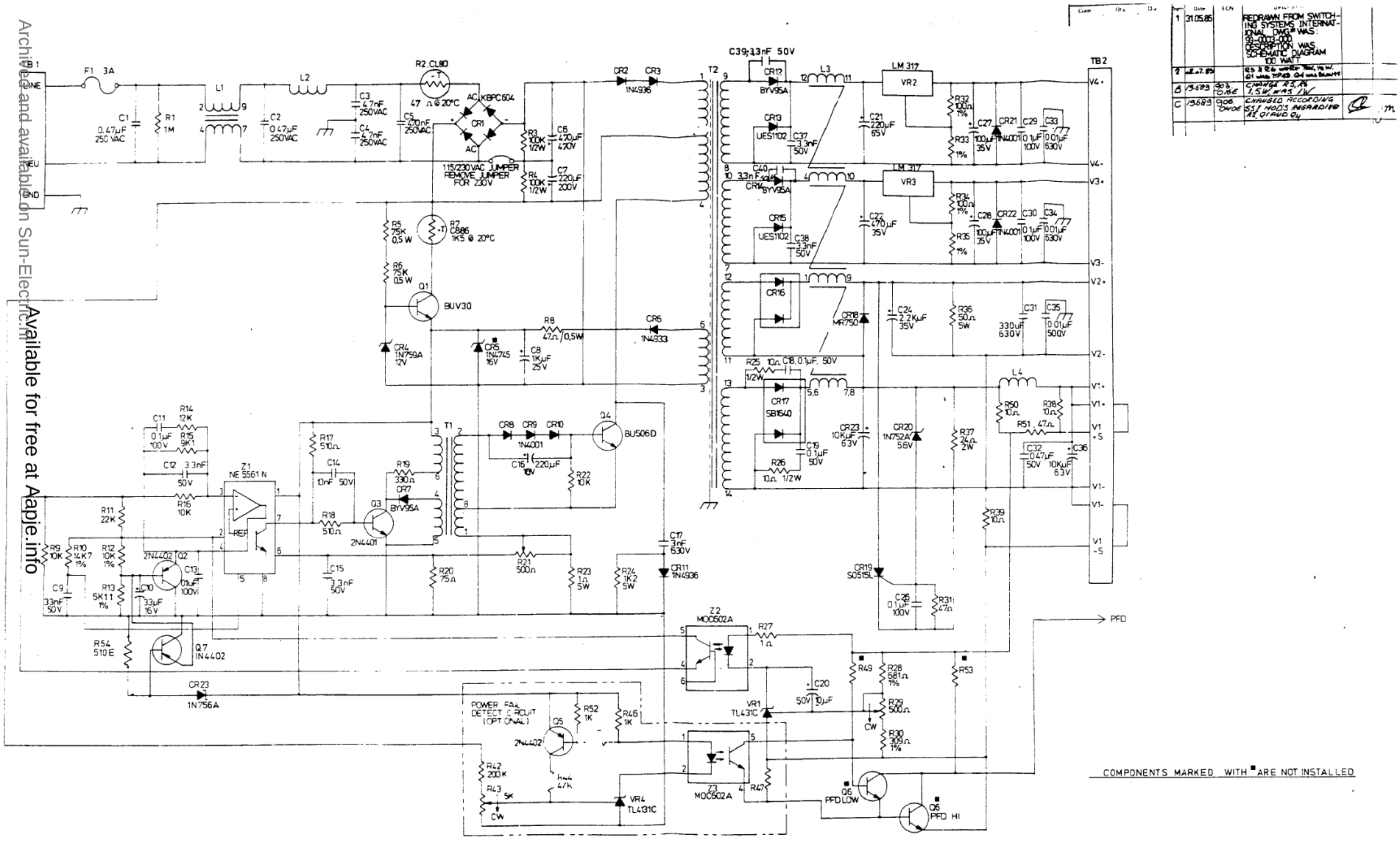
Scale		Date	Used in MCS 2000
Designed by			Material
Drawn by	R. v.d. HOEF	30-07-91	
Checked by	Peter Tol	17-9-91	
Approved	Roman Dar	18.9.91	Finish

Unless otherwise specified: Dimensions are in mm. Tolerances on: Angles ± 0.5 Holes ± 0.1 Rest ± 0.5

Remove all sharp corners and remove burrs

Description	REMOTE CONTROL ASS'Y II	Dwg. No	7009E9316.54
SUN ELECTRIC EUROPE BV	A2	Sheet 1 of 1	Issue A
		Code -	
		Project no. E9134	

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COMPONENTS MARKED WITH ■ ARE NOT INSTALLED

Item	Date	ECN	
1	31.05.85		REDRAWN FROM SWITCHING SYSTEMS INTERNATIONAL DWG.# WAS: 90-00003-000 DESCRIPTION WAS: SCHEMATIC DIAGRAM 100 WATT
2	18.07.89		R5 & R6 wattage changed from 1/2W, 0.1 watt to 75K 0.5 watt was 68K 1/4W
B	13.09.89	903 0365	CHANGED R3,R4 1.5W WAS 1W
C	19.09.89	906 0406	CHANGED ACCORDING SSI 100S UPGRADING M. GRAUD Q4

SUN REF ASSY 7009E9310_32 REV C
7009E9005

Ref. SSI Ass'y no.: 50-0003-001
Serial no. 4665 or higher.

Scale		Date	Name: Used on Sun 2011, Sun MC32000.
Drawn by	Tjin A See M.	31.05.85	
Checked by	R. Lammers	06.07.89	
Approved	J.P. Martin	06.07.89	

SCHEMATIC SYSTEM POWER SUPPLY, SSI, 100WATT

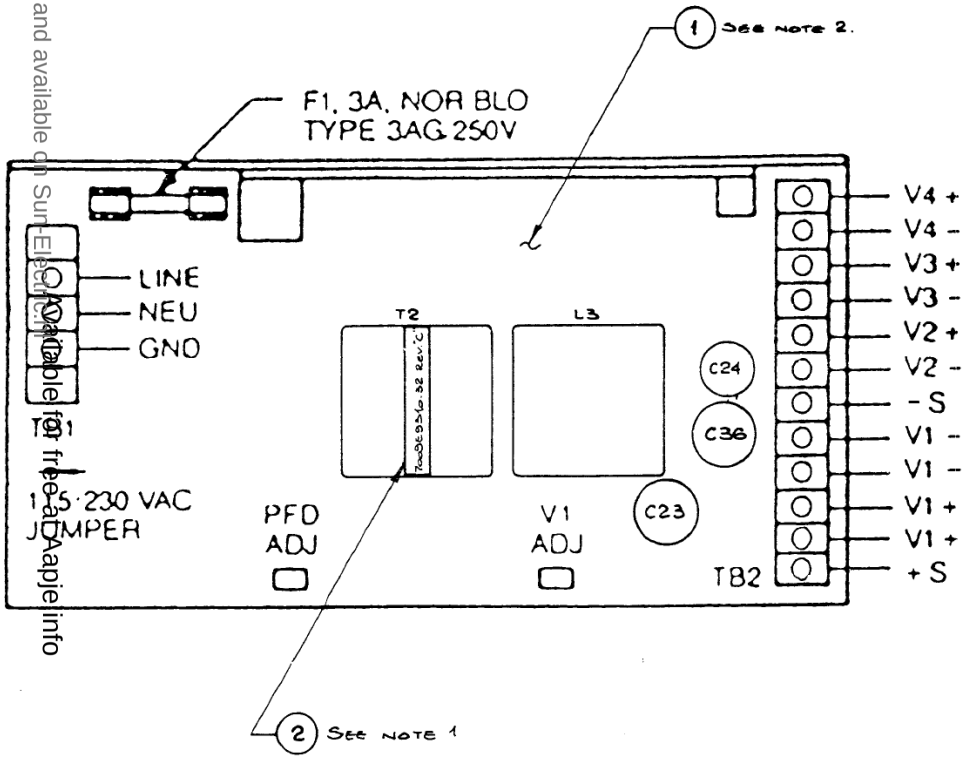
7092E9025

Sun ELECTRIC EUROPE AMSTERDAM

A1

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REVISIONS					
SYM	DATE	ECN	DESCRIPTION	CHECK	APPR.
C	26.06.89	—	ERN # 0308		



NOTES: 1. STICK LABEL, 7009E9310-32 Rev."C", ON TRANSFORMER T2 AS SHOWN.

2. MAKE SURE SSI SERIE NO. IS 4665 OR HIGHER.

Item	Qty.	Dwg./Part no	Description	Remarks
2	1	0003-0673-563	LABEL, ADHESIVE (7009E9310-32 Rev."C")	
1	1	7009E9005	POWER SUPPLY UNIT SSI	

Scale	—	Date	Used in MCS 2000
Designed by			Material
Drawn by	TJIN A SOE M.	27.06.89	
Checked by	R. LAMMERS	060789	
Approved	G.H.T. Manten	06.07.89	Finish

Unless otherwise specified: Dimensions are in mm.; Tolerances on: Angles ± 0,5° Holes ± 0,1 Rest ± 0,5

Remove all sharp corners and remove burrs

Description: SWITCHING PSU ASS'Y

Dwg. no. 7009E9310-32

SUN ELECTRIC EUROPE B.V.

Auteursrecht voorbehouden volgens de wet

A3

Sheet 1 of 1

Code

Project no. E8904

Issue C

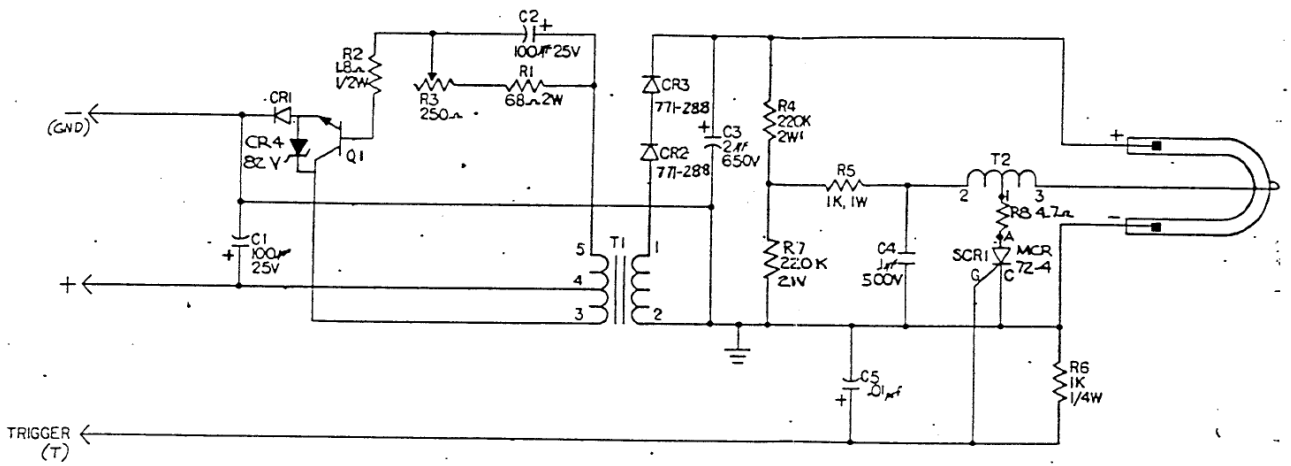
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LIST OF MATERIAL

QTY REQD	PART NO.	DESCRIPTION	ITEM NO.

LAST NO. USED
R8, C5, CR4, T2, Q1, SCR1



REF. ASSY NO. B 5745
REF. PCB NO. C5747

SYM	DATE	REVISIONS	ECN	APVL
2				
1				

(DO NOT SCALE) TOLERANCES (EXCEPT AS NOTED)

ANGLES ±
FRACTIONS ±
DECIMALS .000 ± .005
.00 ± .015
.0 ±

Sun ELECTRIC CORPORATION
CHICAGO, ILLINOIS 60631 U.S.A.

TITLE: SCHEMATIC -TIMING LIGHT

MODEL: SUN 2014

MAT'L AND/OR FINISH

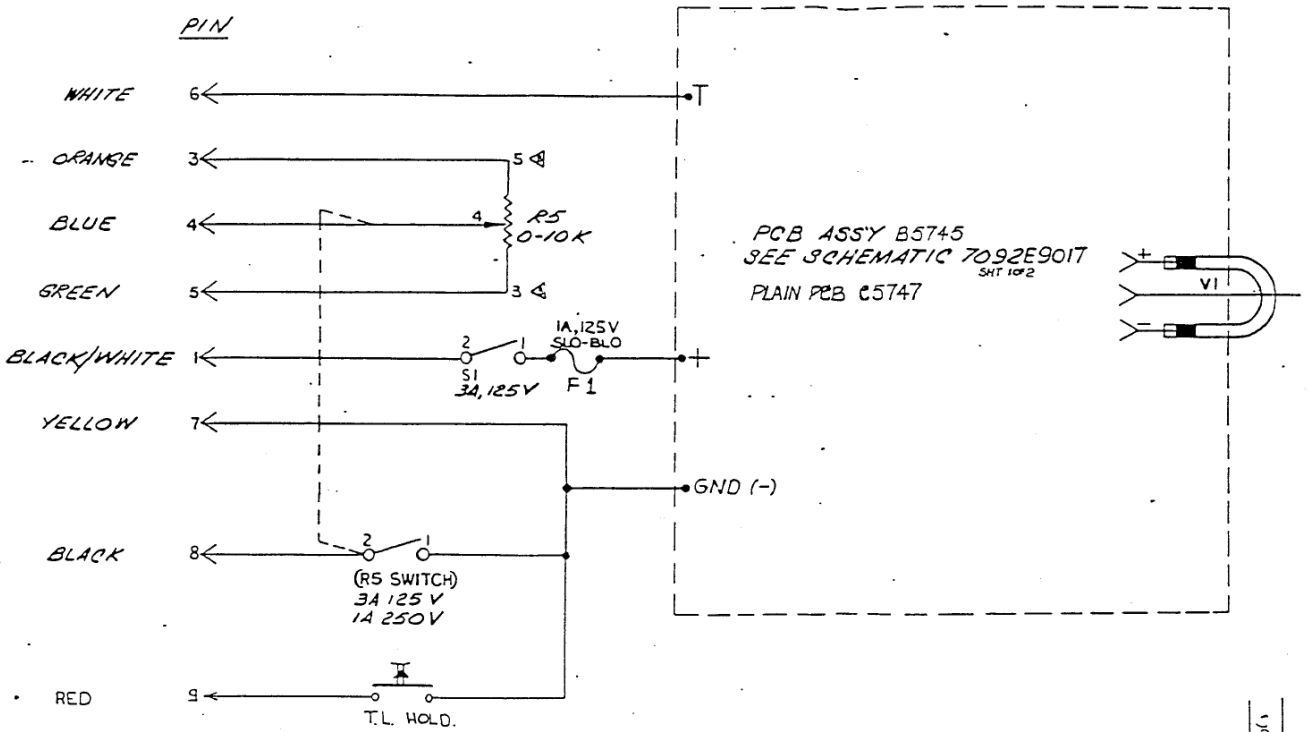
DWG BY L.A.P. 3-16-78 ENG APVL ____/____/____

CHK BY ____ 10/4/85 ENG APVL ____/____/____

SCALE | SHT 1 OF 2 | DWG SIZE C | DWG NO 7092E9017

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LIST OF MATERIAL			
QTY REQD	PART NO.	DESCRIPTION	ITEM NO.



SYM	DATE	REVISIONS	ECN	APVL

(DO NOT SCALE) TOLERANCES (EXCEPT AS NOTED)

ANGLES ± DECIMALS .000 ± .005 .00 ± .015

FRACTIONS ± 0 ±

SUN ELECTRIC CORPORATION
CHICAGO, ILLINOIS 60631 U.S.A.

TITLE: SCHEMATIC TIMING LIGHT

MODEL: SUN-2014

MAT'L AND/OR FINISH

DWG BY SH 1-5-75 ENG APVL

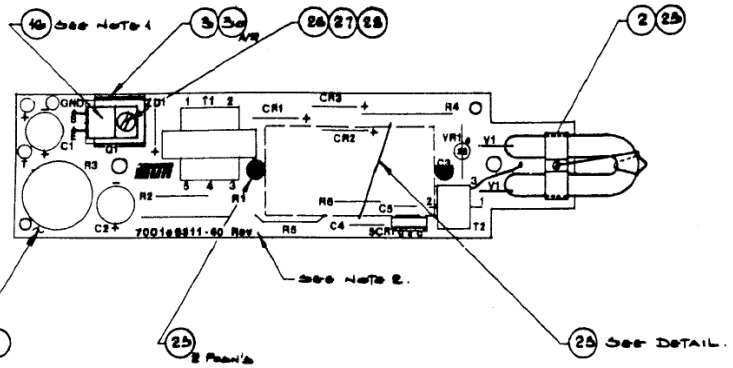
CHK BY ENG APVL

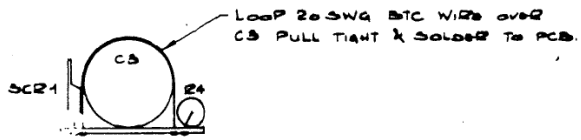
SCALE | SHT 2 OF 2 | DWG SIZE C | DWG NO. 7092E9017

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Revisions					
Rev	DATE	ECN	DESCRIPTION	CHECK	APPR.
B	Feb '89	—	ECN # 2261	P.T.	BJ





Scrap view Showing Method of fixing C5 To Board.

LINE NR	DIRECT ASSEM PART NR	QUAN.	COMPONENTS & SUB ASSEMBLIES	B/M PAGE NR ITEM NR.
1	7025E9310-60	1	Printed Circuit Board	
2	5923-0003-000	1	Trigger Clip	
3	0776-0937-000	1	Heatsink (Base mat. is 4cm²	
4			of Al. sht 0003-0612-659)	
5	0003-0680-750	1	Resistor 68R 10% 2W	R1
6	0003-0680-756	1	Resistor 1R8 10% .5W	R2
7	0003-0680-755	1	Resistor 22OK 10% 2W	R4
8	0003-0680-642	1	Resistor 1K 5% .25W	R6
9	0680-1169-000	1	Resistor 1K 5% 1W	R3
10	0685-0377-000	1	Pots. 250R 20% 3W	R5
11	0778-0394-000	1	Transformer inverter	T1
12	0778-0405-001	1	Transformer trigger	T2
13	0003-0771-565	1	Diode zener 82V	ZD1
14	0771-0283-000	1	Diode fast recovery	CR1
15	0771-0288-000	2	Diode 800V 1A	CR2 CR3
16	0776-0226-000	1	Transistor NPN power	Q1
17	1677-0011-000	1	Flash tube Xenon	V1
18	0859-0067-000	1	Regulator Gas. Disch. Tube	VR1
19	0003-0679-693	2	Capacitor 100µF 25V Elec.	C1 C2
20	0860-0070	1	Capacitor 0.1µF 500V	C4
21	0860-0097-000	1	Capacitor 0.01µF 100V	C5
22	0679-0455-000	1	Capacitor 2µF 650V	C3
23	0003-0637-610	150mm	Wire bare 20SWG	
24	0003-0606-572	3	Terminal pin	
25	0609-0093-000	3	Eyelet 5/32 MAD	
26	0404-0308-523	1	Screw M3*8 PAN HD.	
27	0409-0300-103	1	Nut M3 HEX	
28	0400-0300-203	1	Washer M3 INT.S/P	
29	0771-0317-000	1	SCR MRC-72-6	SCR1
30	0626-0541	A/R	Heatsink Compound	
31	7092E9017	ref	Schematic Timing Light	
32				
33				
34				
35				
36				
37				
38				
39				
40				

NOTES: 1. CUT BACK MIDDLE PIN (C) OF POWER TRANSISTOR.

2. STAMP OR WRITE CURRENT REVISION LEVEL.

Item	Qty	Dwg / Part no	Description		Remarks
Scale 1 : 1			Date	Used in Sun2a14, Sam4aaa, Mac8a-a	
Designed by				Material	
Drawn by M.Tijn A. Boer			19.05.89		
Checked by Peter Tal			20.01.89		
Approved			21.3.89	Finish	

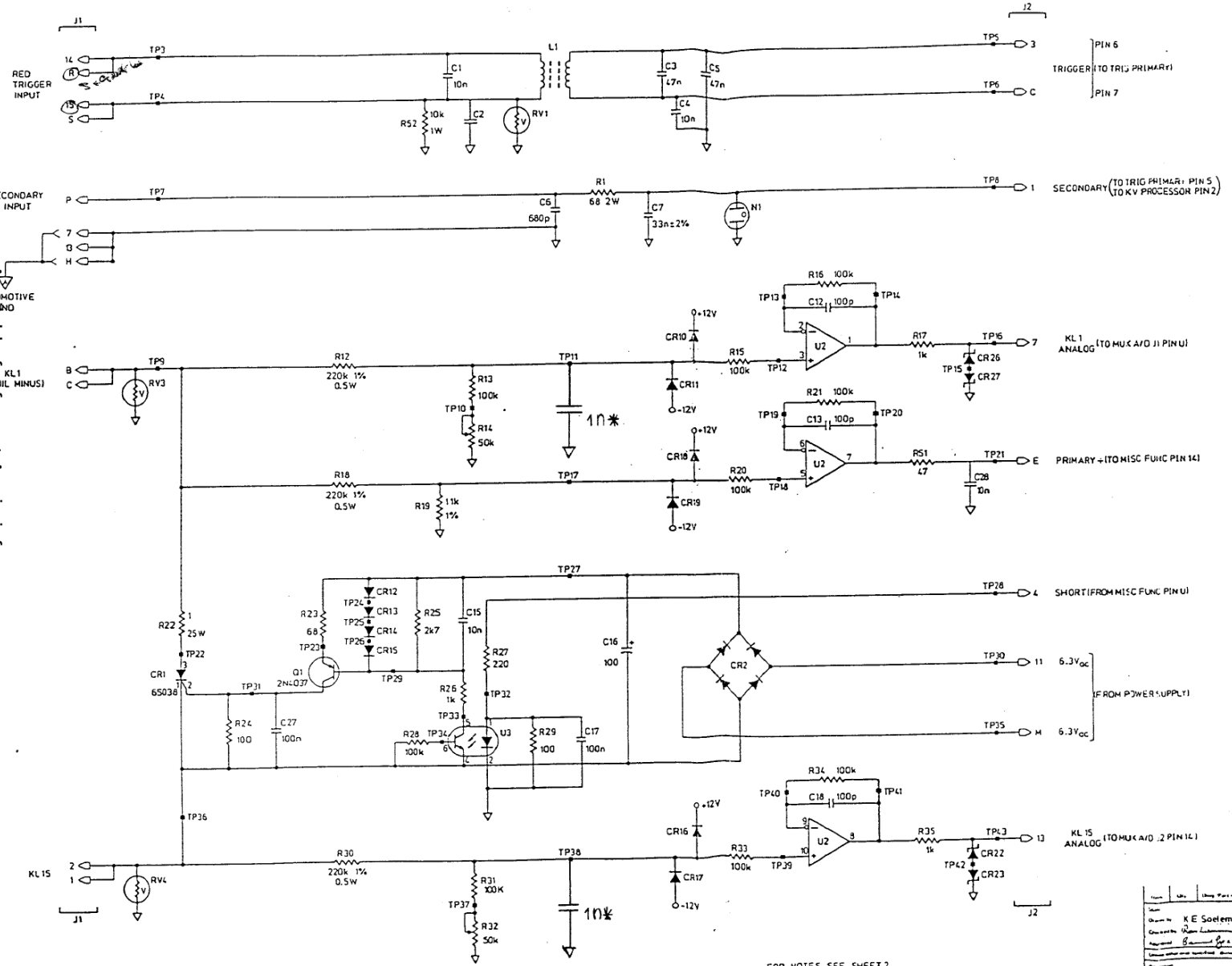
Unless otherwise specified: Dimensions are in mm. Tolerances on Angles ± 0.5 Holes ± 0.1 Rest ± 0.5

Remove all sharp corners and remove burrs 7001E9311-60

Description PRINTED CIRCUIT BOARD ASSEMBLY Timing Light — Dwg no 7001E9311-60

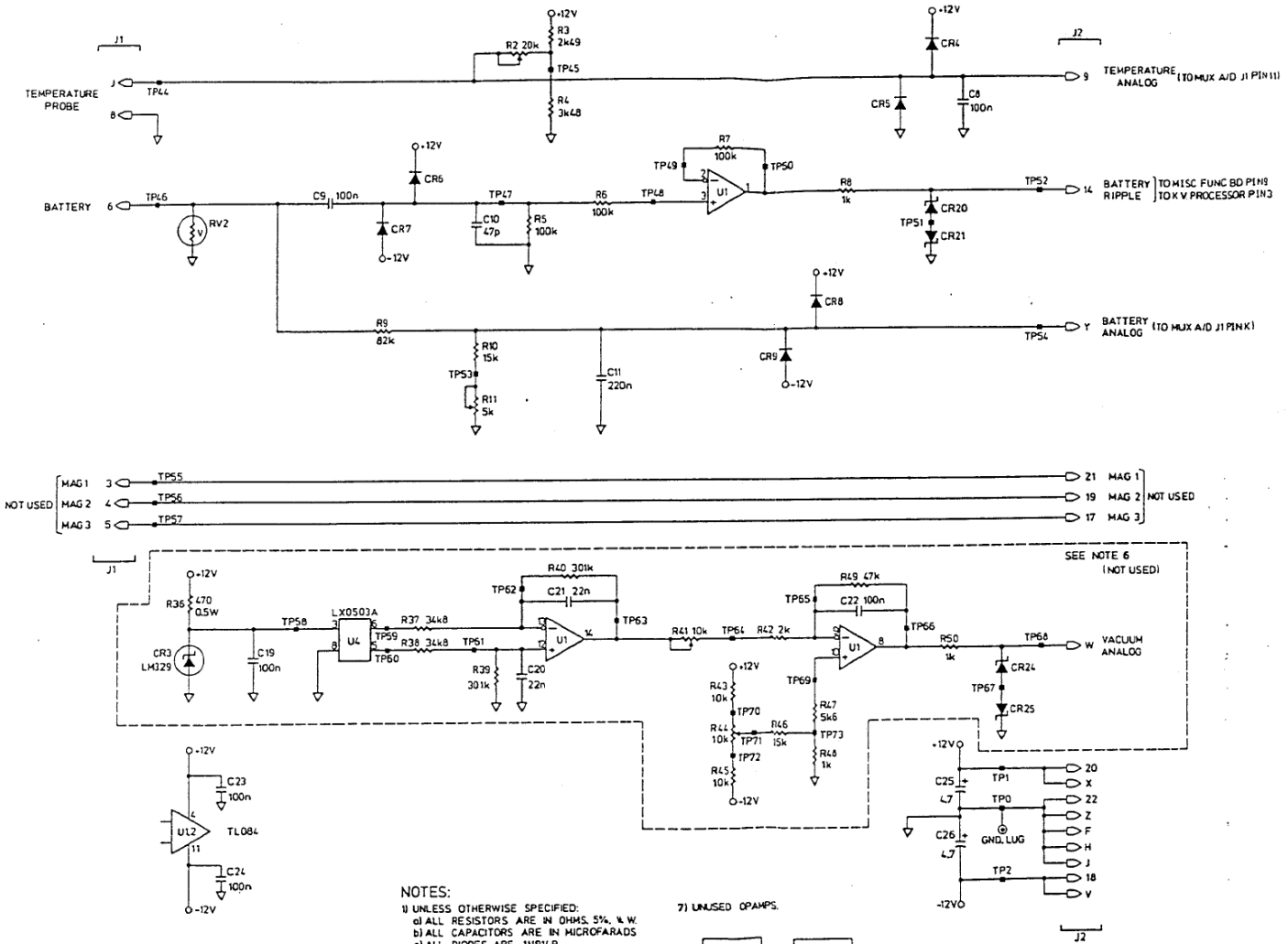
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A2 — Sheet 1 of 1 — Code — Project no. — Issue B



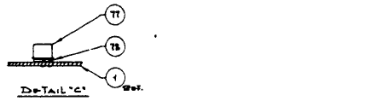
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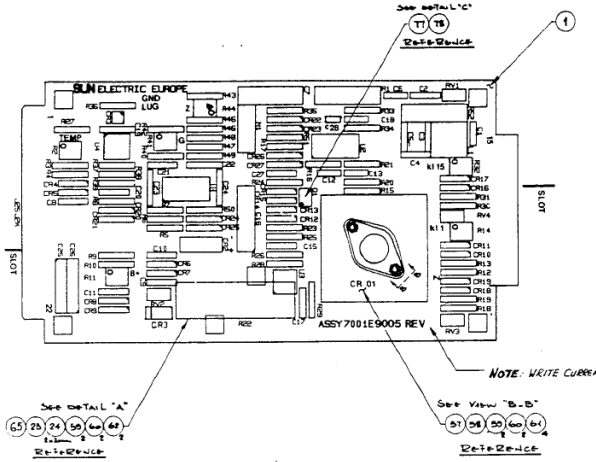
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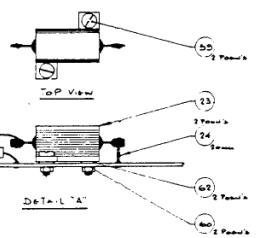


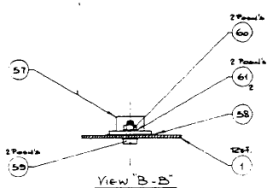
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Revisions					
Sym	Date	ECN	Description	Check	Appd
A	06-88	—	[illegible]	P.T.	[illegible]
B	06-89	3.06.0235	ADDED ITEM 65	G.K.	[illegible]
C	12-89	9.11.081E	ADDED "NOTE: WRITE CURRENT REV LEVEL BEHIND REV"	P.T.	[illegible]









Item	Qty.	Dwg./Part No.	Description	Ref. Designation
78	1	0005.0776.551	PAD	Q1
77	1	0776.0198.000	TRANSISTOR 2N 4037	Q1
76				
75				
74				
73	4	0745.0208.000	VOLT DEPENDANT RESISTOR 275V	RV1 - RV4
72				
71				
70	1	0775.0385.000	TOROID TRANSFORMER	L1
69				
68				
67	6	0803.5755.000	DIODE ZENER 6.8V ½W	CR24-28, CR26-27
66	16	0771.0272.000	DIODE 1N5914B	CR4-CR19
65	1	0771.0246	DIODE 1N5624	CR3
64				
63	1	0774.0061.000	RECTIFIER BRIDGE MDA 220A-2	CR2
62	2	0460.0300.000	WASHER M3 NYLON	R22
61	4	0460.0300.003	WASHER M3 INT. S/P.	CR1
60	4	0460.0300.100	NUT M3 FULL	CR1, R22
59	4	0404.0068.525	SCREW M3x8 Pos Pan Head	CR1, R22
58	1	0776.0302.000	Mica Washer	CR1
57	1	0771.0266.000	THYRISTOR (65 Amps)	CR1
56				
55				
54	1	0389.0061.000	Neon Bulb	N1
53				
52	1	0778.0128.000	INTEGRATED CIRCUIT, OPTO-COUPLER	U8
51	2	0005.0776.647	INTEGRATED CIRCUIT, TL 084CN	U1, U2

50				
49				
48	1	0005.0670.676	CAPACITOR MET. POLY. .01µF, 250V	C1
47	3	0670.0464.000	CAPACITOR CER. DISC. 1nF, 2KV	C4, C15, C28
46	1	0005.0670.619	CAPACITOR CER. DISC. 68pF, 1KV	C6
45	3	0005.0670.705	CAPACITOR CER. DISC. 1nF,	C12, C13, C18
44	1	0005.0670.746	CAPACITOR CER. 47pF	C10
43	1	0005.0670.627	CAPACITOR MET. POLY, .68µF, 250V	C11
42	6	0005.0670.668	CAPACITOR MET. POLY, .1µF, 100V	C8, C9, C17, C21, C23
41				C24
40	2	0005.0670.758	CAPACITOR CER. 47nF, 1KV, Y5U	C3, C5
39	1	0005.0670.749	CAPACITOR POLY. 33nF, 630V	C7
38				
37				
36	1	0670.0258.000	CAPACITOR ELEC., 1000µF, 25V	C16
35	2	0005.0678.744	CAPACITOR ELEC., 4.7µF, 25V	C20, C26
34				
33				
32				
31	5	0005.0501.000	RESISTOR ZERO OHM	R20, R40, R47, R48, R49
30				
29	2	0685.0565.000	RESISTOR VARIABLE 50K	R44, R52
28	1	0685.0411.000	RESISTOR VARIABLE 20K	R2
27	1	0005.0685.548	RESISTOR VARIABLE 5K	R11
26				
25				
24	1 metre	0005.0681.611	WIRE TINNED COPPER 22AWG	R22
23	1	0005.0681.558	RESISTOR 12 5% 25W	R22
22	1	0005.0686.761	RESISTOR 10K 5% 1W	R52
21	1	0686.0736.000	RESISTOR 68Ω 10% 2W	R1
20	5	0005.0676.614	RESISTOR 22K 1% ½W	R12, R18, R30, R31, R32
19				
18				
17	1	1670.1104.000	RESISTOR 11K 1% ½W	R19
16	1	1670.2453.000	RESISTOR 845Ω 1% ½W	R4
15	1	1670.2403.000	RESISTOR 2K40 1% ½W	R6
14				
13	12	0686.2401.000	RESISTOR 100K 5% ½W	R9, R17, R26, R33, R34, R35, R36, R37, R38, R39, R50, R51
12				
11	1	0686.2401.000	RESISTOR 82K 5% ½W	R29
10	1	0686.2275.000	RESISTOR 15K 5% ½W	R40
9	1	0686.2261.000	RESISTOR 2K7 5% ½W	R23
8	4	0686.2243.000	RESISTOR 1K 5% ½W	R5, R27, R24, R25
7	1	0686.2247.000	RESISTOR 22Ω 5% ½W	R21
6	2	0686.2218.000	RESISTOR 100Ω 5% ½W	R24, R225
5	1	0686.2268.000	RESISTOR 68Ω 5% ½W	R28
4	1	0686.2241.000	RESISTOR 47Ω 5% ½W	R31
3				
2				
1	1	700 2BE 3015	PCB SIGNAL INPUT	

Item	Qty.	Dwg./Part No.	Description	Ref. Designation

Scale: 1:1	Drawn: Tim A. Jee M.	Date: 4.8.88	Material: Used on Sun 2e14, Sun 4e0 MCA 2000.
Approved:	Peter Tel	11.05.88	
Released:	Bernard Gee	17.5.88	

PRINTED CIRCUIT BOARD ASS'Y
SIGNAL INPUT

700 1E 3005

Sun | A1 | Sheet 1 of 1 | E8713 | C

Ref. B/MP 0613C/34
Ref Screen # 700 2E 3016

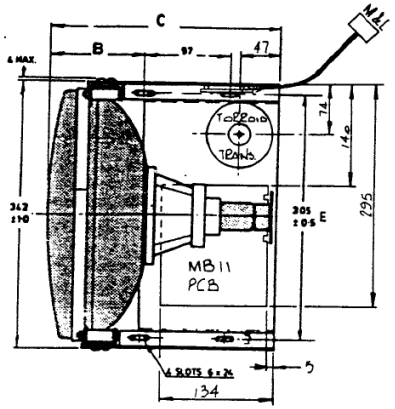
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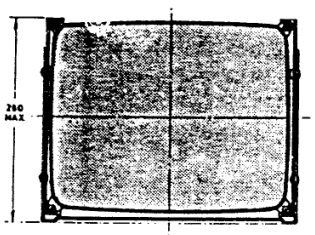
Hole Schedule		
Code	Qty	Dia

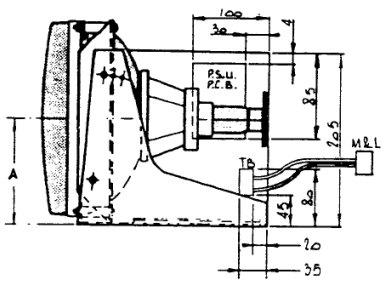
Revisions					
Sym	Date	ECN	Description	Check	Appr
A	—	—	—		
B	24.11.87	—	ERN # 0137 R6618TOR 4K7 WAS 1002	S.T.	BG

C.R.T. Angle	Dimensions A	B	C
0°	136	126	294

NOTE 1. Allow a tolerance of ± 2·0 on dims. A.B.& C.
NOTE 2. For CRTs with a bonded safety panel add 5·0 to dimensions B.& C.
NOTE 3. Chassis material. STEEL. Finish. ZINC PLATE.
NOTE 4. SPECIAL Metalwork can be supplied as follows:-
1. With CRT Angle at 5° & Dim. A at 147 (110°crt)
2. With CRT Angle at 10° & Dim. A at 150 (110°crt) in this instance Dim. E is 304.







All dimensions are in millimetres.

1.1 GENERAL SPECIFICATION

	28mm
CRT SIZE	15"
CRT ANGLE	110°
CRT PHOSPHOR	P-31
POWER *	110V/220V
LINE FREQUENCY	15- 22KHz
VERTICAL FREQUENCY	50- 60Hz
RESOLUTION AT CENTRE	1200 LINES
LINEARITY	≤ 2%
EHT TYPICAL	17KV
LINE BLANKING	11- 7uS
VERT BLANKING	750uS
VIDEO INPUT UNTERMIYATED	12K
TERMINATED	4K7
VIDEO RESPONSE	35MHz
VIDEO RISE/FALL	10nS
VIDEO WHITE +ve	2.75V
LINE SYNC +ve	2.5- 5V
VERT SYNC -ve or +ve	2.5- 6uS 2.5- 5V 10- 500uS

CONTROLS. CONTRAST, BRIGHTNESS, V.HOLD, H. HOLD, H. AMP, H, LIN, GEN LIN, BOTT LIN, V. AMP, FOCUS, SET FH, HF ADJ, V.SHIFT.

STORAGE TEMPERATURE RANGE.	-20°C - +75°C
OPERATING TEMPERATURE RANGE.	0°C - +55°C
OPERATING ALTITUDE.	10,000ft max
WEIGHT (BOARD AND SCAN COIL).	1.0kg
DIMENSIONS.	See board drawings

MFG.: KME
TYPE/PART No.: SEE DWG. NO.

* * INDICATES PREWIRED FOR 110V OPERATION!

Item	Qty	Dwg. Part no.	Description	Matl. Spec	Remarks
Scale N.T.S.			Date	Remarks USED ON SUN 2014 & MCS 2000	
Drawn by T.J.N.A.Sce M			20.01.87		
Checked by Peter Tal			26.04.88		
Approved Ronnie Egan			26.4.88	Finish	

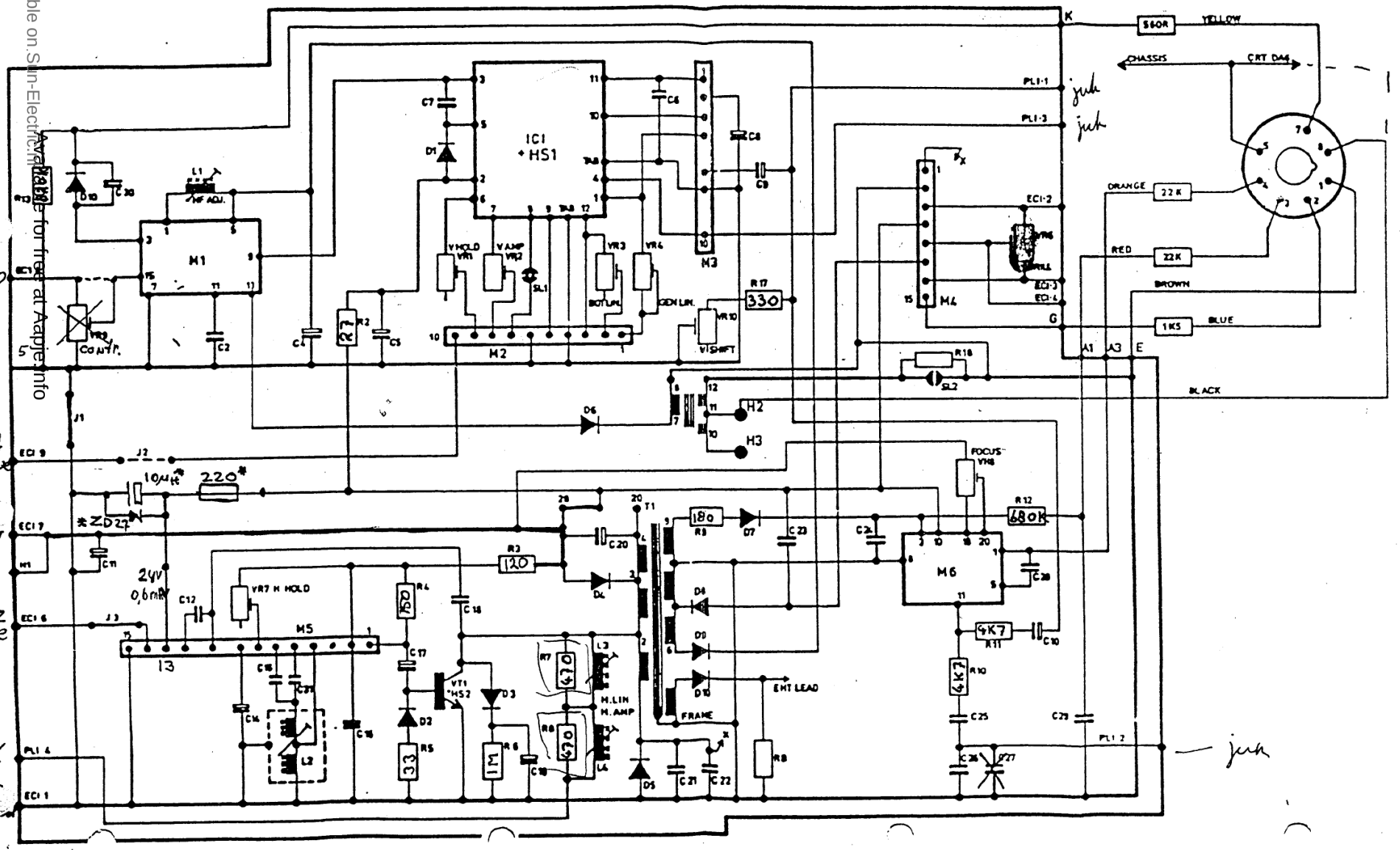
Unless otherwise specified: Dimensions in mm. Tolerances ± 0.5 mm. Angles ± 1°.

MONITOR. MOD. KME MC-1500 | 700-9E9313-10

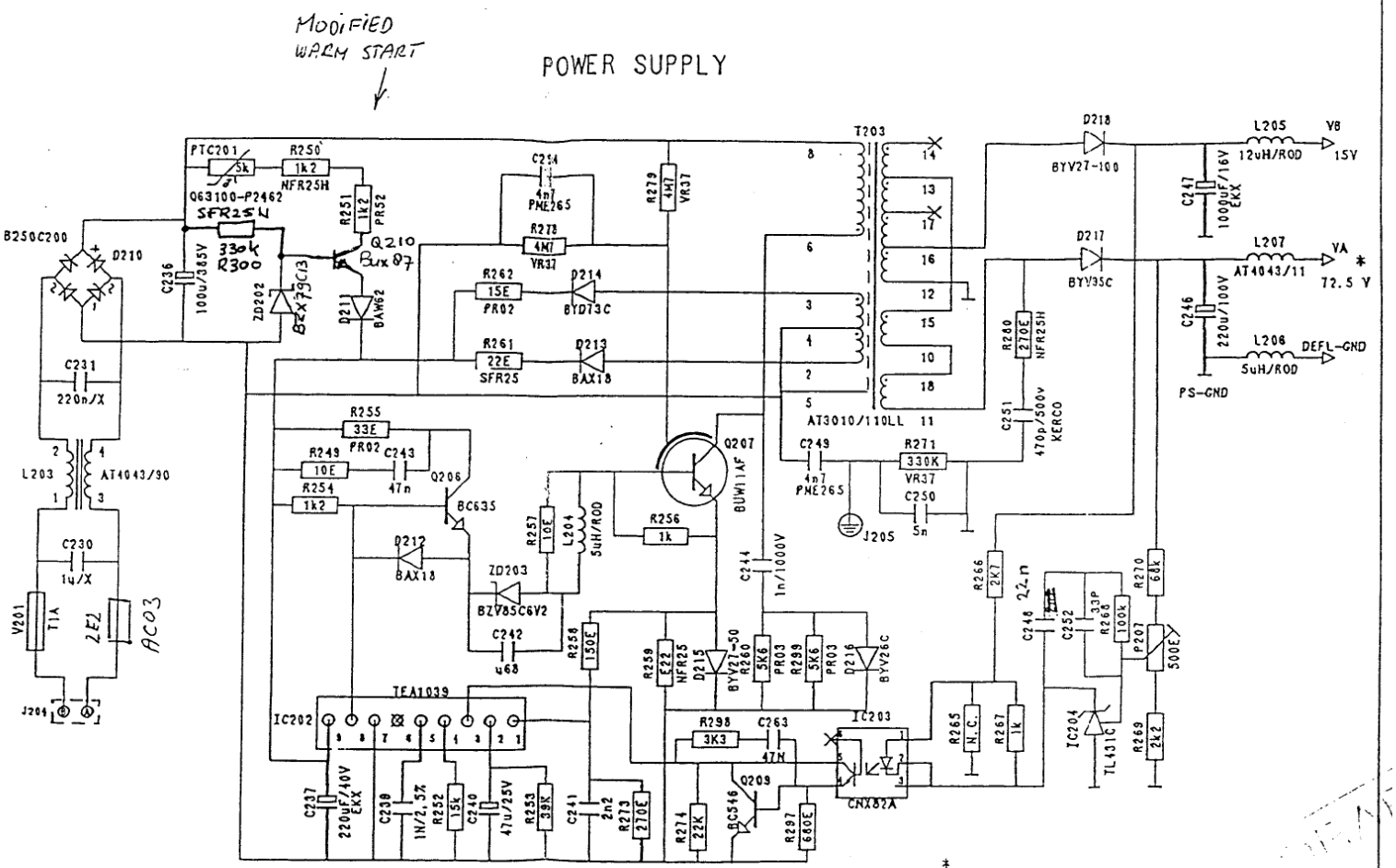
Sun | A2 | Sheet 1 of 1 | Issue B

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Let op, aarde CRT vast aan kwart op D van de CRT voet



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VA = 72.5 V when an AMS deflection-coil is used.
VA = 69 V when an ELDOR deflection-coil is used.

C263 D229 IC205 J208
L207 PIC201 P211 Q209
R239 T204 V201 ZD204

Mounted raised:
NFR25 / NFR25H
PR XX

UNSPECIFIED RESISTORS:
E24 VALUES = SFR16T
E96 VALUES = MRS16T OR BEYSLAG MBA0204-508X

SUN

REV:	DATE:	
REV:	DATE:	

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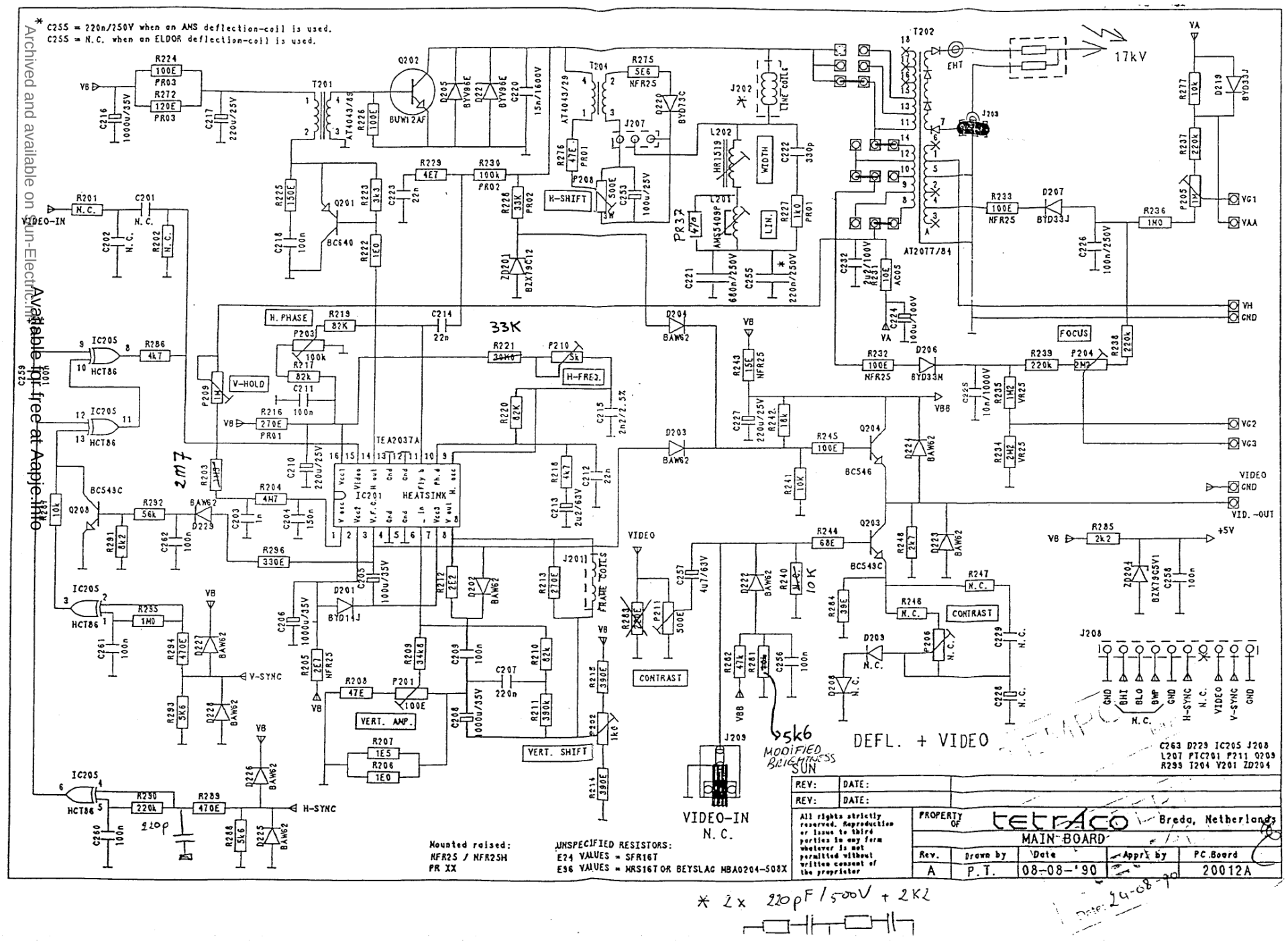
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MAIN BOARD

Rev.	Drawn by	Date	Appr. by	PC\Board
A	P.T.	08-08-'90		20012A

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* C255 = 220n/250V when an ANS deflection-coil is used.
C255 = N.C. when an ELDOR deflection-coil is used.



REV:	DATE:				
REV:	DATE:				

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PROPERTY OF tetraco Breda, Netherlands

MAIN-BOARD

Rev.	Drawn by	Date	Appr. by	PC.Board
A	P.T.	08-08-'90		20012A

* 2x 220pF/500V + 2K2

Date: 24-08-90

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SECTION 5

SPARE PARTS AND ACCESSORIES

SUN ELECTRIC EUROPE B.V.

BILL OF MATERIAL

NAME : TIMING LIGHT ASSEMBLY

PART.NR.: 700939015-00

MAJOR ASSEMBLY:

MODELNR: SUN2014,SAM4000, MCS2000

ASSEMBLY DWG: 7009E9015-00

REF.NR.: PC

WIRING DIAC:

ERN: 0261

DATE : MARCH 1989

SHEET: 1 OF 1

LINE NR	DIRECT ASSEM PART NR	QUAN./	COMPONENTS & SUB ASSEMBLIES	B/M ITEM NR.	PAGE NR
1	7054-0021-01	1	LENS HOLDER (MOULDED)		
2	709639055-73	1	LABEL-TY		
3	7059-0406-00	1	TUBE LIGHT HOUSING		
4	3406-0134-00	2	SCREW, 6-32*1/4 F.H.		
5	3764-0207-00	1	ROCKER SWITCH		
6	3685-0360-00	1	RESISTOR VARIABLE W.AC SW		
7	0610-0162-00	1	SCREW, #8*1,F.HD TYPE25		
8	7003-0341-00	1	PLATE, MTG CONTROL		
9	7015-0059-00	1	TUBE REFLECTOR		
10	7096E9059-21	1	LENS OBJECTIVE		
11	2035-0201-00	1	STRAIN RELIEF		
12	4055-0187-00	1	OVERLAY PLATE		
13	700939315-12	1	MOD. HOUSING ASS'Y		
14	6004E9310-04	1	TIMING LIGHT LEAD ASS'Y		
15	3160-0161-00	1	SCREW #8*5/8 F.HD TYPE25		
16	3602-0035-00	1	LOCKWASHER,3/8 INT.		
17	3409-0029-00	1	NUT, 3/8-32 HEX		
18	404-0408-223	2	SCREW M4*8mm,CSK HD		
19	7009-1063-00	1	KNOB ASSEMBLY		
20	3686-0022-00	2	SET SCREW,6-32*1/8		
21	003-1001-011	2	SPACER M4*8mm,18mm LG		
22	404-0408-533	2	SCREW, M4*8mm PZ HD		
23	400-0400-203	2	LOCKWASHER M4		
24	7001E9311-60	1	TIMING LIGHT PCB ASS'Y		
25	003-0689-563	1	SWITCH		
26	0663-0333-02	150mm	WIRE RED 20 AWG		
27	0663-0333-09	280mm	WIRE WHITE 20 AWG		
28	0669-0196-00	135mm	TUBING, HEATSHRINK		
29	0626-0026-00	A/R	ADHESIVE		
30	7092E9017-00	REF	SCHEMATIC TIMING LIGHT		
31					
32					
33					
34					
35					
36					
37					
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39					
40					

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SUN ELECTRIC EUROPE B.V.

RECOMMENDED SPARE PARTS LIST FOR THE MCS 2000SL AND OCS 2000SL

PART NO:	QTY: MCS	OCS	DESCRIPTION
7009E9313-75	1	1	CARD RACK MODULE
7001E9008	1	1	DIGITAL BACKPLANE CCA
7001E9010	1	1	DIGITAL I/O CCA REV. C
700lE9011	1	1	KV CARD READER CCA
7001E9012	1	1	MUX A/D CCA
7001E9311-19	1	1	CENTRONICS INTERFACE CCA
700lE9311-48	1	1	ERAM CCA
7001E9311-44	1	1	ECPU68K CCA (NEW & DIGISCOPE)
7001E9311-54	1	1	DIGITAL SCOPE CCA
7001E9310-05	1	1	FLOPPY DISIURS-232 CCA
7001E9311-59	1	1	ECRT CONTROLLER CCA
7001E9009	1	1	PRE-PROCESSOR CCA
700lE9016	1	1	ANALOG BACKPLANE CCA
7001E9020	1	1	KV SLOPE CCA
7001E9310-44	1	1	KV PROCESSOR CCA
700lE9311-57	1	1	KV PROCESSOR CCA (DIGISCOPE)
700lE9044	1	1	VOLT/OHM CCA
7001E9311-56	1	1	VOLT/OHM CCA (DIGISCOPE)
7001E9310-12	1	1	AMPS CCA
700lE9045	1	1	TIMING CCA
7001E9017	1	1	MISC. FUNCTION CCA
700lE9019	1	1	TRIGGER PRIMARY
7001E9311-55	1	1	TRIGGER PRIMARY CCA (DIGISCOPE)
7009E9314-81	1	1	DIGITAL MONITOR ASSY (20" VDU)
7096E4055-92	1	1	TUBE 20”
7001E9311-51	1	1	MONITOR CCA
7009E9314-84	1	1	DEFLECTION COIL (20” VDU)
7001E9311-50	1	1	POWER SUPPLY CCA
7009E9314-82	1	1	TORODIAL TRANSFORMER ASSY

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SUN ELECTRIC EUROPE B.V.

PART NO:	QTY: MCS	OCS	DESCRIPTION
TEST LEADS:			
.....			LABEL OCS REM. CONTR.
4600E9309-89	1		LABEL MCS REM. CONTR.
7009E9316-54	1		REMOTE CONTROL ASSY (MCS)
7009E9316-62		1	REMOTE CONTROL ASSY (OCS)
6004E9311-22	1	1	REMOTE CONTROL CABLE
7010E9310-83	1	1	REMOTE CONTROL KEYPAD
0865-0112	1	1	REMOTE CONTROL MAGN. STRIP (2x)
7054-0102	1	1	REMOTE CASE, UPPER
7054-0103	1	1	REMOTE CASE, LOWER
7009E9015	1	1	TIMING LIGHT ASSY
6004E9310-32	1	1	TEST HARNESS UNIVERSAL
6005-0133	2	2	TEST LEAD ASSY CURRENT
4720-0000-000	1	1	TEST LEAD PATTERN
4721-0000-000	1	1	TEST LEAD TRIGGER
1747-0101-000	2	2	PATTERN PICK-UP
0507-0006-000	2	2	TRIGGER PICK-UP
6004E9005-000	1	1	TEST LEAD ASSY VOLT/OHM
6004E9004-000	1	1	TEST LEAD ASSY TEMP LOW
6006-0003	1	1	HOSE ASSY VACUUM
MISCELLANEOUS CCAS;			
7001E9005	1	1	SIGNAL INPUT CCA
7001E9311-60	1	1	TIMING LIGHT CCA
POWER SUPPLIES:			
7009E9310-32	1	1	SWITCHING POWER SUPPLY ASSY
7009E9313-79	1	1	MAINS TRANSFORMER ASSY

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PART NO:	QTY: MCS	OCS	DESCRIPTION
MISCELLANEOUS ELECTRICAL:			
0531-0003-000	1	1	FILTER RF INTERFERENCE
0003-0689-574	1	1	HEADSIGN SWITCH
0003-0689-574	1	1	TESTER ON/OFF SWITCH
0003-0689-542	1	1	ROCKER SWITCH PUMP ON/OFF
7009E9311-64	1	1	DISK DRIVE
0739-0039	5	5	MAINS FUSES (5 AMP)
1922-0106-021	2	2	CIRCUIT BREAKER (8 AMP) BOOM
0587-0504-000	2	2	FAN AXIAL 115V
0003-0909-529	2	2	FESTON LAMP 12V 5W
0003-0910-524	1	1	HEADSIGN BALLAST RESISTOR
0003-0910-536	2	2	HEADSIGN LAMP
TESTER ACCESSORIES:			
0003-2000-609	2	2	TEST PROBE RED
0003-2000-608	2	2	TEST PROBE BLACK
0003-2000-614	2	2	CROC CLIP RED
0003-2000-613	2	2	CROC CLIP BLACK
3676-A	1	1	SPARK PLUG CONNECTOR SET
7096E4026	1	1	BOSCH ADAPTER KIT
4107-0000-000	1	1	AUTOLITE ADAPTOR 6MM
4108-0000-000	1	1	AUTOLITE ADAPTOR 5MM
4344-000	1	1	RESISTANCE TEST CONTACTOR
0002-0133-015	1	1	JUMPER LEAD
7096E9056-23	5	5	AIR FILTER
0002-1028-000	1	1	HT PLIERS
0647-0170	1	1	TEE ASSY HOSE
6004E9006-000	1	1	SHORTING OUT FAN LEAD

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